19-2848; Rev 1; 11/03

EVALUATION KIT AVAILABLE

Highly Integrated Level 2 SMBus Battery Charger

MAX1535A

General Description

The MAX1535A is a highly integrated, multichemistry battery charger that simplifies construction of advanced smart chargers with a minimum number of external components. It uses Intel's system management bus (SMBus) to control the charge voltage, charge current, and the maximum current drawn from the AC adapter. High efficiency is achieved through use of a constant off-time step-down topology with synchronous rectification.

In addition to support of the Smart Battery Charger Specifications Rev 1.1, the MAX1535A includes additional features. The maximum current drawn from the AC adapter is programmable to avoid overloads when supplying the load and the battery charger simultaneously. This enables the user to reduce the cost of the AC adapter. The MAX1535A provides a digital output that indicates the presence of an AC adapter. Based on the presence or absence of the AC adapter, the MAX1535A automatically selects the appropriate source for supplying power to the system by controlling two external P-channel MOSFETs. Under system control, the MAX1535A allows the battery to undergo a relearning or conditioning cycle in which the battery is completely discharged through the system load and then recharged.

The MAX1535A is capable of charging 2, 3, or 4 lithium-ion (Li+) cells in series, providing charge currents as high as 8A. The DC-to-DC converter in the MAX1535A uses a high-side P-channel switch with an N-channel synchronous rectifier. The charge current and input current-limit sense amplifiers have low input-offset errors and can use small-value sense resistors (0.01Ω, typ).

The MAX1535A is available in a 5mm x 5mm 32-pin thin QFN package and operates over the extended -40°C to +85°C temperature range. An evaluation kit is available to reduce design time.

Applications

Notebook and Subnotebook Computers

Tablet PCs

Portable Equipment with Rechargeable Batteries

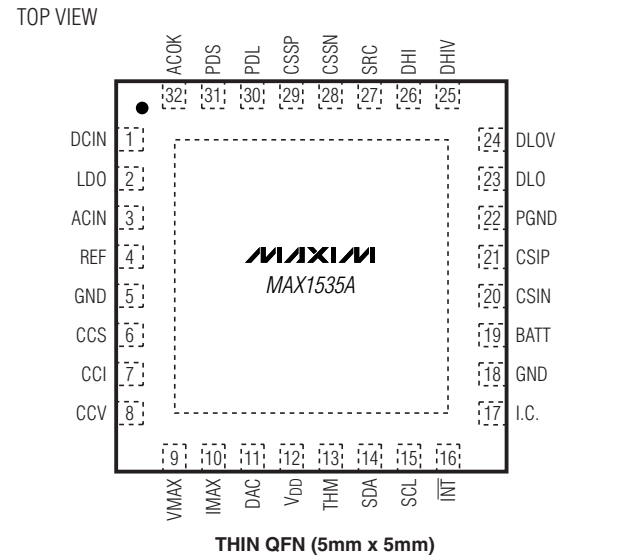
Features

- ♦ **Compliant with Level 2 Smart Battery Charger Specifications Rev 1.1**
- ♦ **Intel SMBus 2-Wire Serial Interface**
- ♦ **±0.5% Charge-Voltage Accuracy**
- ♦ **11-Bit Charge-Voltage Resolution**
- ♦ **±3% Input Current-Limit Accuracy**
- ♦ **Uses Small (10mΩ) Current-Sense Resistors**
- ♦ **8A Maximum Charge Current**
- ♦ **6-Bit Input and Charge-Current Resolution**
- ♦ **8V to 28V Input Voltage Range**
- ♦ **175s Charge Safety Timer**
- ♦ **Automatic Selection of System Power Source**
- ♦ **Charges any Battery Chemistry (Li+, NiCd, NiMH, Lead Acid, etc.)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1535AETJ	-40°C to +85°C	32 Thin QFN (5mm x 5mm)

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Highly Integrated Level 2 SMBus Battery Charger

ABSOLUTE MAXIMUM RATINGS

DCIN, CSSP, CSSN, SRC, ACOK to GND .....-0.3V to +30V
DHIV to SRC .....-6V to +0.3V
DHI, PDL, PDS to GND .....-0.3V to V_{SRC} + 0.3V
BATT, CSIP, CSIN to GND .....-0.3V to +20V
CSIP to CSIN, or CSSP to CSSN .....-0.3V to +0.3V
CCI, CCS, CCV, DAC, REF to GND .....-0.3V to V_{LDO} + 0.3V
V_{DD}, ACIN, SCL, SDA, DLOV, LDO, THM, $\overline{INT}$, IMAX, VMAX to GND .....-0.3V to +6V
DLOV to LDO .....-0.3V to +0.3V
DLO to PGND .....-0.3V to V_{DLOV} + 0.3V
PGND to GND .....-0.3V to +0.3V
LDO Short-Circuit Current 50mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 21.3mW/°C above +70°C) ...1702mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION					
Charge-Voltage Accuracy	ChargeVoltage() = 0x41A0 and 0x3130	-0.5		+0.5	%
	ChargeVoltage() = 0x20D0	-0.8		+0.8	
	ChargeVoltage() = 0x1060	-1.0		+1.0	
Full-Charge Voltage	ChargeVoltage() = 0x41A0	16.716	16.800	16.884	V
	ChargeVoltage() = 0x3130	12.529	12.592	12.655	
	ChargeVoltage() = 0x20D0	8.332	8.400	8.468	
	ChargeVoltage() = 0x1060	4.150	4.192	4.234	
CHARGE-CURRENT REGULATION					
CSIP-to-CSIN Full-Scale Current-Sense Voltage	V_{BATT} = 12V	76.60	80.64	84.67	mV
Compliance Current Accuracy	10mΩ sense resistor (R2 in Figure 1) between CSIP and CSIN; ChargeCurrent() = 0x1F80	-5		+5	%
Charge Current	10mΩ sense resistor (R2 in Figure 1) between CSIP and CSIN; ChargeCurrent() = 0x1F80	7.660	8.064	8.467	A
	10mΩ sense resistor (R2 in Figure 1) between CSIP and CSIN; ChargeCurrent() = 0x0080		128		mA
BATT/CSIP/CSIN Input Voltage Range		0		19	V
CSIP/CSIN Input Current	V_{DCIN} = 0V, or charger not switching		0.1	1.0	µA
	V_{CSIP} = V_{CSIN} = 12V		300	700	
INPUT-CURRENT REGULATION					
CSSP-to-CSSN Full-Scale Current-Sense Voltage	V_{DCIN} = 18V	104.5	110.0	115.5	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current-Limit Accuracy	10mΩ sense resistor (R1 in Figure 1) between CSSP and CSSN; InputCurrent() = 0x1580 (11.008A)	-5		+5	%
	10mΩ sense resistor (R1 in Figure 1) between CSSP and CSSN; InputCurrent() = 0x1000 (8.192A)	-3		+3	
	10mΩ sense resistor (R1 in Figure 1) between CSSP and CSSN; InputCurrent() = 0x0800 (4.096A)	-6.5		+6.5	
	POR (InputCurrent() = 0x0080)		256		mA
CSSP/CSSN Input Voltage Range		8		28	V
CSSP/CSSN Input Current	V_{DCIN} = 0V		0.1	1.0	µA
	V_{CSSP} = V_{CSSN} = V_{DCIN} > 8.0V		300	750	
SUPPLY AND LINEAR REGULATOR					
DCIN Input Voltage Range		8		28	V
DCIN Undervoltage Lockout Trip Point	DCIN falling	7.0	7.4		V
	DCIN rising		7.50	7.85	
DCIN Quiescent Current	8V < V_{DCIN} < 28V		2.7	6.0	mA
BATT Input Current	V_{BATT} = 19V, V_{DCIN} = 0V, or charger not switching		0.1	1.0	µA
	V_{BATT} = 2V to 19V, V_{DCIN} > V_{BATT} + 0.3V		200	500	
LDO Output Voltage	8V < V_{DCIN} < 28V, no load	5.25	5.40	5.50	V
LDO Load Regulation	0 < I_{LDO} < 10mA		34	100	mV
LDO Undervoltage Lockout Trip Point	V_{DCIN} = 8V	3.20	4.00	5.15	V
V_{DD} Range		2.7		5.5	V
V_{DD} UVLO Rising Threshold			2.5	2.7	V
V_{DD} UVLO Hysteresis			100		mV
V_{DD} Quiescent Current	V_{DCIN} < 6V, V_{DD} = 5.5V, V_{SCL} = V_{SDA} = 5.5V		17	27	µA
REFERENCE					
REF Output Voltage	0 < I_{REF} < 500µA	4.083	4.096	4.109	V
REF Undervoltage Lockout Trip Point	REF falling		3.1	3.9	V
TRIP POINTS					
BATT POWER_FAIL Threshold	V_{DCIN} falling	50	100	150	mV
BATT POWER_FAIL Threshold Hysteresis		100	200	300	mV
ACIN Threshold	ACIN rising	1.966	2.048	2.130	V
ACIN Threshold Hysteresis		10	20	30	mV
ACIN Input Bias Current	V_{ACIN} = 2.048V	-1		+1	µA

Highly Integrated Level 2 SMBus Battery Charger

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING REGULATOR					
Off-Time	V_{BATT} = 16.0, V_{DCIN} = 21.0	540	600	660	ns
	V_{BATT} = 19.0, V_{DCIN} = 21.0	230	270	310	
DLOV Supply Current	ChargerMode() = 0x0001		5	10	µA
Maximum Discontinuous Mode Peak Current			0.5		A
Battery Undervoltage Charge Current	V_{BATT} = 2.6V per cell		128		mA
DHIV Output Voltage	With respect to SRC	-4.5	-5.0	-5.5	V
DHIV Sink Current		10			mA
DHI On-Resistance Low	V_{DHI} = V_{DHIV}, I_{DHI} = -10mA		4	7	Ω
DHI On-Resistance High	V_{DHI} = V_{SRC}, I_{DHI} = 10mA		1	3	Ω
DLO On-Resistance High	V_{DLOV} = 4.5V, I_{DLO} = 100mA		4	7	Ω
DLO On-Resistance Low	V_{DLOV} = 4.5V, I_{DLO} = -100mA		1	3	Ω
ERROR AMPLIFIERS					
GMV Transconductance	ChargeVoltage () = 0x41A0, V_{BATT} = 16.8V	0.0625	0.1250	0.2500	µA/mV
GMI Transconductance	ChargeCurrent () = 0x1F80, V_{CSIP} - V_{CSIN} = 80.64mV	0.5	1	2	µA/mV
GMS Transconductance	InputCurrent () = 0x1580, V_{CSSP} - V_{CSSN} = 110.08mV	0.5	1	2	µA/mV
CCI Clamp Voltage	0.25V < V_{CCI} < 2.0V	150	300	600	mV
CCV Clamp Voltage	0.25V < V_{CCV} < 2.0V	150	300	600	mV
CCS Clamp Voltage	0.25V < V_{CCS} < 2.0V	150	300	600	mV
ACOK					
ACOK Input Voltage Range		0		28	V
ACOK Sink Current	V_{ACOK} = 0.4V, ACIN = 1.5V	1			mA
ACOK Leakage Current	V_{ACOK} = 28V, ACIN = 2.5V			1	µA
PDS, PDL SWITCH CONTROL					
PDS Switch Turn-Off Threshold	DCIN with respect to BATT, DCIN falling	50	100	150	mV
PDL Switch Turn-On Threshold	DCIN with respect to BATT, DCIN falling	50	100	150	mV
PDS Switch Threshold Hysteresis	DCIN with respect to BATT		200		mV
PDL Switch Threshold Hysteresis	DCIN with respect to BATT		200		mV
PDS Output Low Voltage, PDS Below SRC	I_{PDS} = 0V	8	10	12	V
PDS Turn-On Current	PDS = SRC	6	12		mA
PDS Turn-Off Current	V_{PDS} = V_{SRC} - 2V, V_{DCIN} = 16V	10	50		mA
PDL Turn-On Resistance	PDL = GND	50	100	150	kΩ
PDL Turn-Off Current	V_{CSSN} - V_{PDL} = 1.5V	6	12		mA
PDL and PDS Transition Delay Time	PDS and PDL are unloaded	4	10	15	µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PDL-to-PDS Switchover Time in Relearn Mode	PDS and PDL are unloaded	4	10	16	µs
MAXIMUM CHARGE-VOLTAGE SETTING					
V_{BATT} to V_{VMAX} Ratio	V_{MAX} = 2V, ChargeVoltage () = 0x4B00	4.95	5.0	5.05	V/V
V_{MAX} Input Voltage Range		0		V_{REF}	V
V_{MAX} Input Bias Current	0 < V_{VMAX} < V_{REF}			1	µA
MAXIMUM CHARGE-CURRENT SETTING					
I_{CHARGE} to V_{IMAX} Ratio	V_{IMAX} = 0.8V, ChargeCurrent () = 0x1F80	4.75	5	5.25	A/V
IMAX Input Voltage Range		0		V_{REF}	V
IMAX Input Bias Current	0 < V_{IMAX} < V_{REF}			1	µA
THERMISTOR COMPARATOR					
Thermistor Overrange Threshold	V_{DD} = 2.7V to 5.5V, THM falling	89.5	91	92.5	% of V_{DD}
Thermistor Cold Threshold	V_{DD} = 2.7V to 5.5V, THM falling	73.5	75	76.5	% of V_{DD}
Thermistor Hot Threshold	V_{DD} = 2.7V to 5.5V, THM falling	21.5	23	24.5	% of V_{DD}
Thermistor Underrange Threshold	V_{DD} = 2.7V to 5.5V, THM falling	3.5	5	6.5	% of V_{DD}
Thermistor Comparator Hysteresis	All four comparators, V_{DD} = 2.7V to 5.5V		50		mV
SMBus INTERFACE LEVEL SPECIFICATIONS (V_{DD} = 2.7V TO 5.5V)					
SDA/SCL Input Low Voltage	V_{DD} = 2.7V to 5.5V			0.8	V
SDA/SCL Input High Voltage	V_{DD} = 2.7V to 5.5V	2.1			V
SDA/SCL Input Bias Current	V_{DD} = 2.7V to 5.5V	-1		+1	µA
SDA, $\overline{INT}$ Output Sink Current	VSDA = 0.4V	6			mA
$\overline{INT}$ Output High Leakage Current	$V_{\overline{INT}}$ = 5.5V			1	µA
$\overline{INT}$ Output Low Voltage	$I_{\overline{INT}}$ = 1mA		25	200	mV
SMBus TIMING SPECIFICATIONS (V_{DD} = 2.7V TO 5.5V)					
SMBus Frequency		10		100	kHz
SMBus Free Time		4.7			µs
Start Condition Setup Time from SCL		4.7			µs
Start Condition Hold Time from SCL		4			µs
Stop Condition Setup Time from SCL		4			µs
SDA Hold Time from SCL		300			ns
SDA Setup Time from SCL		250			ns
SCL Low Timeout	(Note 1)	25		35	ms

Highly Integrated Level 2 SMBus Battery Charger

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Period		4.7			µs
SCL High Period		4			µs
Maximum Charging Period Without a ChargeVoltage() or ChargeCurrent() Command		140	175	210	s

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION					
Charge-Voltage Accuracy	ChargeVoltage() = 0x41A0 and 0x3130	-1.6		+1.6	%
	ChargeVoltage() = 0x20D0	-1.6		+1.6	
	ChargeVoltage() = 0x1060	-1.8		+1.8	
Full-Charge Voltage	ChargeVoltage() = 0x41A0	16.532		17.068	V
	ChargeVoltage() = 0x3130	12.390		12.794	
	ChargeVoltage() = 0x20D0	8.266		8.534	
	ChargeVoltage() = 0x1060	4.116		4.268	
CHARGE-CURRENT REGULATION					
CSIP-to-CSIN Full-Scale Current-Sense Voltage	V_{BATT} = 12V	72.58		88.70	mV
Compliance Current Accuracy	10mΩ sense resistor (R2 in Figure 1) between CSIP and CSIN; ChargeCurrent() = 0x1F80	-10		+10	%
Charge Current	10mΩ sense resistor (R2 in Figure 1) between CSIP and CSIN; ChargeCurrent() = 0x1F80	7.258		8.870	A
BATT/CSIP/CSIN Input Voltage Range		0		19	V
CSIP/CSIN Input Current	V_{CSIP} = V_{CSIN} = 12V			800	µA
INPUT-CURRENT REGULATION					
CSSP-to-CSSN Full-Scale Current-Sense Voltage	V_{DCIN} = 18V	99		121	mV
Input Current-Limit Accuracy	10mΩ sense resistor (R1 in Figure 1) between CSSP and CSSN; InputCurrent() = 0x1580 (11.008A)	-10		+10	%
	10mΩ sense resistor (R1 in Figure 1) between CSSP and CSSN; InputCurrent() = 0x1000 (8.192A)	-8		+8	
	10mΩ sense resistor (R1 in Figure 1) between CSSP and CSSN; InputCurrent() = 0x0800 (4.096A)	-10		+10	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CSSP/CSSN Input Voltage Range		8		28	V
CSSP/CSSN Input Current	V_{CSSP} = V_{CSSN} = V_{DCIN} > 8.0V			800	µA
SUPPLY AND LINEAR REGULATOR					
DCIN Input Voltage Range		8		28	V
DCIN Undervoltage Lockout Trip Point	DCIN falling	7.0			V
	DCIN rising			7.85	
DCIN Quiescent Current	8V < V_{DCIN} < 28V			8	mA
BATT Input Current	V_{BATT} = 2V to 19V, V_{DCIN} > V_{BATT} + 0.3V			800	µA
LDO Output Voltage	8V < V_{DCIN} < 28V, no load	5.15		5.65	V
LDO Load Regulation	0 < I_{LDO} < 10mA			100	mV
LDO Undervoltage Lockout Trip Point	V_{DCIN} = 8V	3.00		5.35	V
V_{DD} Range		2.7		5.5	V
V_{DD} Quiescent Current	V_{DCIN} < 6V, V_{DD} = 5.5V, V_{SCL} = V_{SDA} = 5.5V			27	µA
REFERENCE					
REF Output Voltage	0 < I_{REF} < 500µA	4.035		4.157	V
REF Undervoltage Lockout Trip Point	REF falling			3.9	V
TRIP POINTS					
BATT POWER_FAIL Threshold	V_{DCIN} falling	60		160	mV
BATT POWER_FAIL Threshold Hysteresis		90		310	mV
ACIN Threshold	ACIN rising	1.966		2.129	V
ACIN Threshold Hysteresis		5		35	mV
SWITCHING REGULATOR					
Off-Time	V_{BATT} = 16.0, V_{DCIN} = 21.0	540		660	ns
	V_{BATT} = 19.0, V_{DCIN} = 21.0	230		310	
DLOV Supply Current	ChargerMode() = 0x0001			10	µA
Battery Undervoltage Charge Current	V_{BATT} = 2.6V per cell	64		192	mA
DHIV Output Voltage	With respect to SRC	-4.4		-5.5	V
DHIV Sink Current		10			mA
DHI On-Resistance Low	V_{DHI} = V_{DHIV}, I_{DHI} = -10mA			7	Ω
DHI On-Resistance High	V_{DHI} = V_{SRC}, I_{DHI} = 10mA			3	Ω
DLO On-Resistance High	V_{DLOV} = 4.5V, I_{DLO} = 100mA			7	Ω
DLO On-Resistance Low	V_{DLOV} = 4.5V, I_{DLO} = -100mA			3	Ω
ERROR AMPLIFIERS					
GMV Transconductance	ChargeVoltage() = 0x41A0, V_{BATT} = 16.8V	0.0625		0.2500	µA/mV

Highly Integrated Level 2 SMBus Battery Charger

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GMI Transconductance	ChargeCurrent() = 0x1F80, V_{CSIP} - V_{CSIN} = 80.64mV	0.5		2	µA/mV
GMS Transconductance	InputCurrent() = 0x1580, V_{CSSP} - V_{CSSN} = 110.08mV	0.5		2	µA/mV
CCI Clamp Voltage	0.25V < V_{CCI} < 2.0V	140		600	mV
CCV Clamp Voltage	0.25V < V_{CCV} < 2.0V	140		600	mV
CCS Clamp Voltage	0.25V < V_{CCS} < 2.0V	140		600	mV
ACOK					
ACOK Input Voltage Range		0		28	V
ACOK Sink Current	V_{ACOK} = 0.4V, ACIN = 1.5V	1			mA
PDS, PDL SWITCH CONTROL					
PDS Switch Turn-Off Threshold	DCIN with respect to BATT, DCIN falling	40		160	mV
PDL Switch Turn-On Threshold	DCIN with respect to BATT, DCIN falling	40		160	mV
PDS Output Low Voltage, PDS Below SRC	I_{PDS} = 0	8		12	V
PDS Turn-On Current	PDS = SRC	6			mA
PDS Turn-Off Current	V_{PDS} = V_{SRC} - 2V, V_{DCIN} = 16V	10			mA
PDL Turn-On Resistance	PDL = GND	40		160	kΩ
PDL Turn-Off Current	V_{CSSN} - V_{PDL} = 1.5V	6			mA
PDL and PDS Transition Delay Time	PDS and PDL are unloaded	4		15	µs
PDL-to-PDS Switchover Time in Relearn Mode	PDS and PDL are unloaded	4		16	µs
MAXIMUM CHARGE-VOLTAGE SETTING					
VMAX Input Voltage Range		0		V_{REF}	V
VMAX to V_{BATT} Ratio	V_{VMAX} = 2V, ChargeVoltage() = 0x4B00	4.9		5.1	V/V
MAXIMUM CHARGE-CURRENT SETTING					
IMAX Input Voltage Range		0		V_{REF}	V
IMAX to I_{CHARGE} Ratio	V_{IMAX} = 0.8V, ChargeCurrent() = 0x1F80	4.5		5.5	A/V
THERMISTOR COMPARATOR					
Thermistor Overrange Threshold	V_{DD} = 2.7V to 5.5V, THM falling	89.5		92.5	% of V_{DD}
Thermistor Cold Threshold	V_{DD} = 2.7V to 5.5V, THM falling	73.5		76.5	% of V_{DD}
Thermistor Hot Threshold	V_{DD} = 2.7V to 5.5V, THM falling	21.5		24.5	% of V_{DD}
Thermistor Underrange Threshold	V_{DD} = 2.7V to 5.5V, THM falling	3.5		6.5	% of V_{DD}
SMBus INTERFACE LEVEL SPECIFICATIONS (V_{DD} = 2.7V TO 5.5V)					
SDA/SCL Input Low Voltage	V_{DD} = 2.7V to 5.5V			0.8	V
SDA/SCL Input High Voltage	V_{DD} = 2.7V to 5.5V	2.15			V
SDA, $\overline{INT}$ Output Sink Current	VSDA = 0.4V	6			mA
$\overline{INT}$ Output Low Voltage	$I_{\overline{INT}}$ = 1mA			200	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{DD} = 3.3V, ACIN = PGND = GND, LDO = DLOV, VMAX = IMAX = REF, C_{LDO} = 1µF, C_{DHIV} = 0.1µF, C_{REF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus TIMING SPECIFICATIONS (V_{DD} = 2.7V TO 5.5V)					
SMBus Frequency		10		100	kHz
SMBus Free Time		4.7			µs
Start Condition Setup Time from SCL		4.7			µs
Start Condition Hold Time from SCL		4			µs
Stop Condition Setup Time from SCL		4			µs
SDA Hold Time from SCL		300			ns
SDA Setup Time from SCL		250			ns
SCL Low Timeout	(Note 1)	25		35	ms
SCL Low Period		4.7			µs
SCL High Period		4			µs
Maximum Charging Period Without a ChargeVoltage() or ChargeCurrent() Command		130		220	s

Note 1: Devices participating in a transfer time out when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).

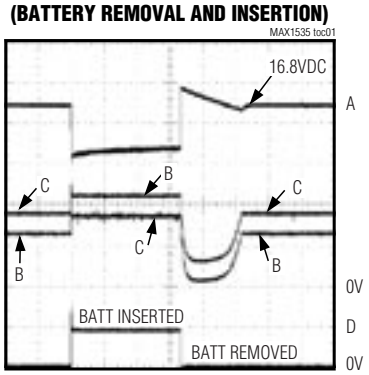
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Highly Integrated Level 2 SMBus Battery Charger

Typical Operating Characteristics

(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

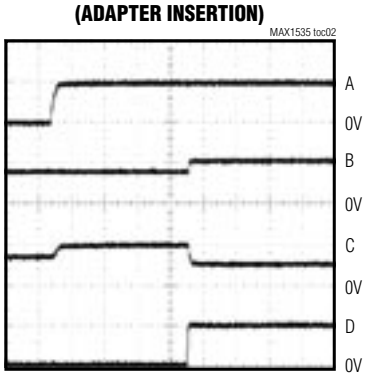
TRANSIENT RESPONSE (BATTERY REMOVAL AND INSERTION)



4ms/div

A: BATTERY VOLTAGE, 500mV/div, AC-COUPLED
B: V_{CCV}, 500mV/div
C: V_{CCI}, 500mV/div
D: CHARGE CURRENT, 2A/div

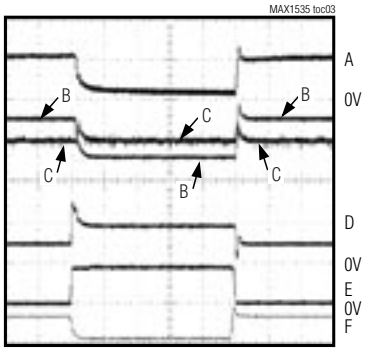
LOAD SWITCH CONTROL (ADAPTER INSERTION)



200µs/div

A: ADAPTER INPUT VOLTAGE, 20V/div
B: V_{CSSN}, 20V/div
C: V_{PDS}, 20V/div
D: V_{PDL}, 20V/div

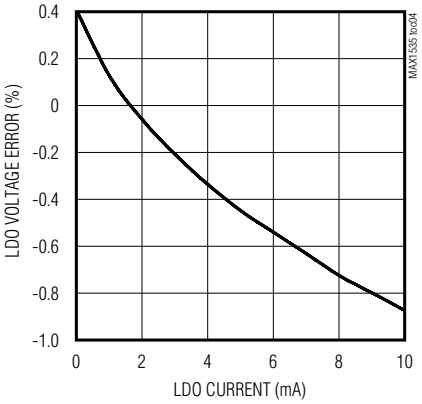
SYSTEM LOAD TRANSIENT



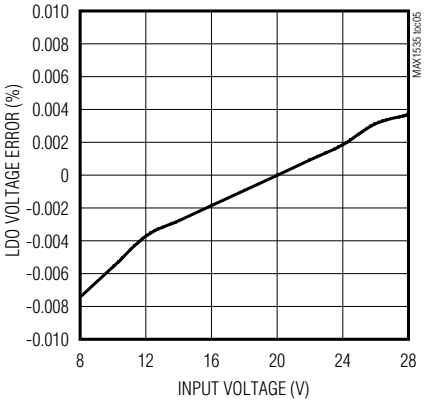
400µs/div

A: V_{BATT}, 500mV/div, AC-COUPLED
B: V_{CCS}, 500mV/div
C: V_{CCI}, 500mV/div
D: AC ADAPTER CURRENT, 5A/div
E: SYSTEM LOAD, 5A/div
F: CHARGE CURRENT, 5A/div

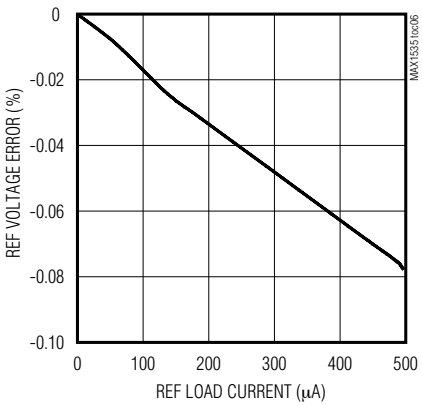
LDO LOAD REGULATION (V_{IN} = 20V)



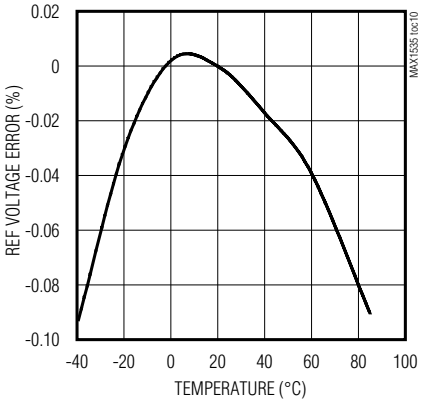
LDO LINE REGULATION



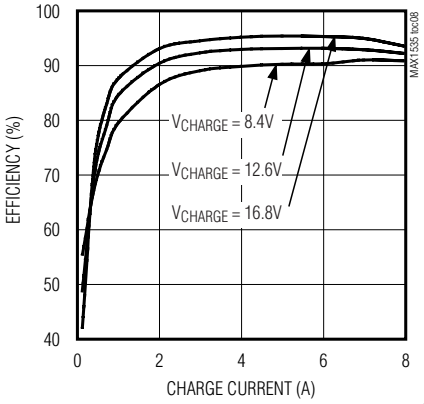
REF LOAD REGULATION



REF VOLTAGE ERROR vs. TEMPERATURE



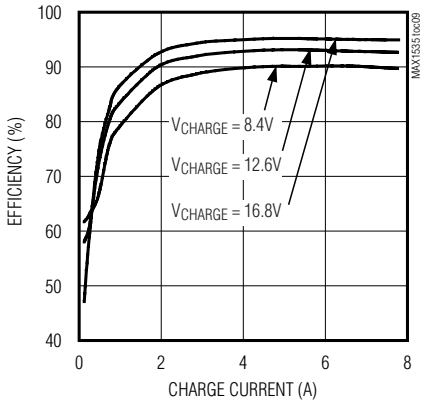
EFFICIENCY vs. CHARGE CURRENT (CONSTANT-VOLTAGE MODE)



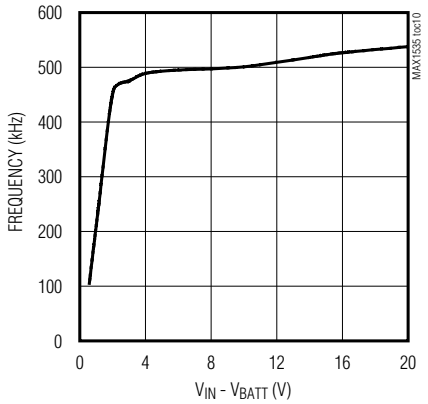
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

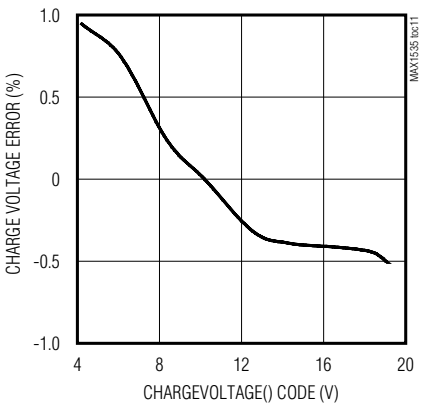
EFFICIENCY vs. CHARGE CURRENT (CONSTANT-CURRENT MODE)



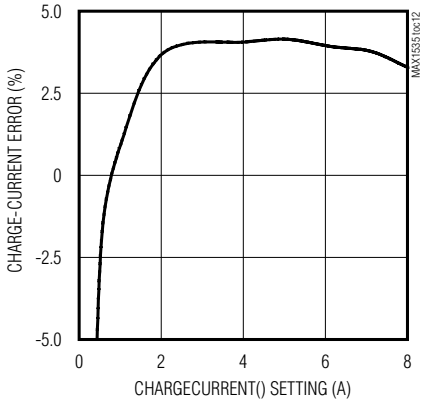
FREQUENCY vs. V_{IN} - V_{BATT}



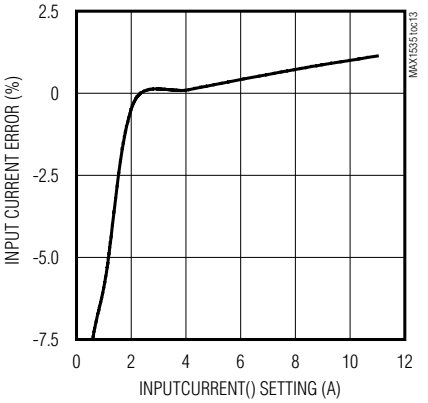
CHARGE-VOLTAGE ACCURACY



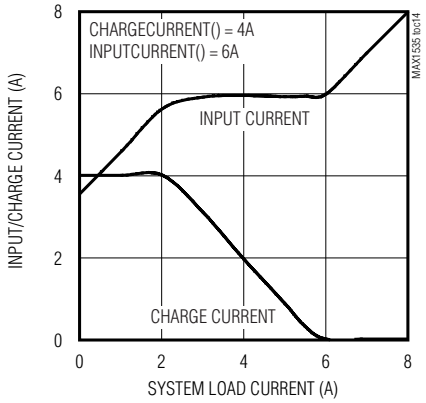
CHARGE-CURRENT ACCURACY



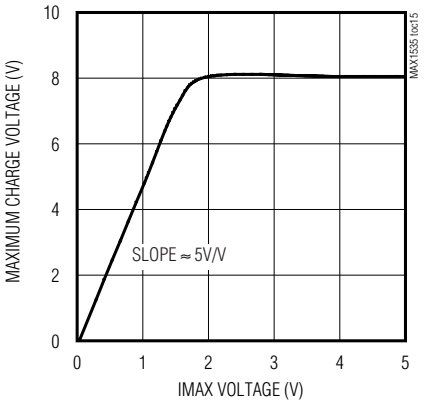
INPUT-CURRENT ACCURACY



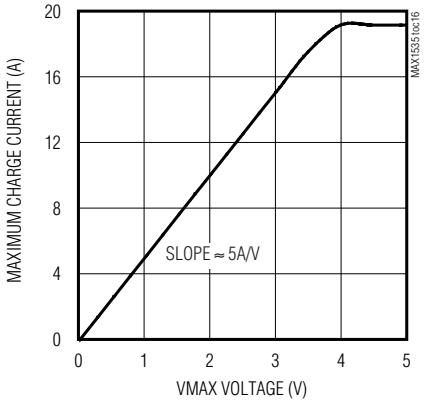
INPUT/CHARGE CURRENT vs. SYSTEM LOAD CURRENT



MAXIMUM CHARGE VOLTAGE vs. IMAX



MAXIMUM CHARGE CURRENT vs. VMAX



Highly Integrated Level 2 SMBus Battery Charger

Pin Description

PIN	NAME	FUNCTION
1	DCIN	DC Supply Voltage Input. Bypass DCIN to power ground (PGND) with a 1µF ceramic capacitor.
2	LDO	5.4V Linear-Regulator Output. The linear regulator powers the internal circuitry of the device. The input of the linear regulator is supplied from DCIN. Bypass LDO with a 1µF ceramic capacitor to GND.
3	ACIN	AC Adapter Detect Input. This uncommitted comparator input can be used to detect if the AC adapter voltage is available for charging.
4	REF	4.096V (Typical) Reference Voltage Output. Bypass REF with a 1µF ceramic capacitor to GND.
5	GND	Analog Ground
6	CCS	Input Current-Limit Regulation Loop Compensation Point. Connect a 0.01µF capacitor to GND.
7	CCI	Charge-Current Regulation Loop Compensation Point. Connect a 0.01µF capacitor to GND.
8	CCV	Charge-Voltage Regulation Loop Compensation Point. Connect a 20kΩ resistor in series with a 0.01µF capacitor to GND.
9	VMAX	Analog Control Input for Setting the Maximum Charge Voltage. The maximum charge voltage can never go above the limit set by VMAX. The ratio of maximum charge voltage to VMAX voltage is 5V/V.
10	IMAX	Analog Control Input for Setting the Maximum Charge Current. The maximum charge current can never go above the limit set by IMAX. The ratio of maximum charge current to IMAX voltage is 5A/V.
11	DAC	DAC Voltage Output. Bypass DAC with a 0.1µF ceramic capacitor to GND.
12	V_{DD}	Logic Circuitry Supply Voltage Input. The voltage range of V_{DD} is 2.7V to 5.5V.
13	THM	Thermistor Voltage Input
14	SDA	SMBus Data Input/Output. SDA is an open-drain output. An external pullup resistor is needed.
15	SCL	SMBus Clock Input. An external pullup resistor is needed.
16	$\overline{INT}$	Interrupt Output. $\overline{INT}$ is an open-drain output. An external pullup resistor is needed.
17	I.C.	Internally Connected Pin. Leave it unconnected or connect it to ground.
18	GND	Analog Ground
19	BATT	Battery Voltage Input
20	CSIN	Negative Input to the Charge Current-Sense Amplifier
21	CSIP	Positive Input to the Charge Current-Sense Amplifier. Connect a 10mΩ current-sense resistor from CSIP to CSIN.
22	PGND	Power Ground
23	DLO	Low-Side Power MOSFET Gate Driver Output. Connect DLO to the gate of the low-side N-channel MOSFET.
24	DLOV	Low-Side Gate Driver Supply. Bypass DLOV with a 0.1µF ceramic capacitor to PGND.
25	DHIV	High-Side Gate Driver Supply. Bypass DHIV with a 0.1µF ceramic capacitor to CSSN.
26	DHI	High-Side Power MOSFET Gate Driver Output. Connect DHI to the gate of the high-side P-channel MOSFET.
27	SRC	Source Connection for PDS and PDL Switch Drivers
28	CSSN	Negative Input to the Input Current-Limit Sense Amplifier
29	CSSP	Positive Input to the Input Current-Limit Sense Amplifier. Connect a 10mΩ current-sense resistor from CSSP to CSSN.
30	PDL	System Load P-Channel MOSFET Switch Driver Output. When the MAX1535A is powered down, the PDL output is pulled to ground through an internal 100kΩ resistor.
31	PDS	Power Source P-Channel MOSFET Switch Driver Output. When the MAX1535A is powered down, the PDS output is pulled to SRC through an internal 1MΩ resistor.
32	ACOK	AC Detect Output. This high-voltage open-drain output is low impedance when ACIN is less than REF/2. The ACOK output remains low impedance when the MAX1535A is powered down.

Detailed Description

The MAX1535A includes all the functions necessary to charge Li+, NiMH, and NiCd smart batteries. A high-efficiency, synchronous-rectified, step-down DC-to-DC converter is used to implement a precision constant-current, constant-voltage charger with input current limiting. The DC-to-DC converter uses an external P-channel MOSFET as the buck switch and an external N-channel MOSFET as the synchronous rectifier to convert the input voltage to the required charge current and voltage. The charge current and input current-limit sense amplifiers have low input-offset errors and can use small-value sense resistors.

The MAX1535A features a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The loops operate independently of each other. The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by the ChargeVoltage() command. The CCI battery current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by the ChargeCurrent() command. The charge current-regulation loop is in control as long as the BATT voltage is below the set point. When the BATT voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. A third loop (CCS) takes control and reduces the charge current when the sum of the system load and the input current to the charger exceeds the power-source current limit set by the InputCurrent() command. The MAX1535A also allows the user to clamp the programmed charge current and charge voltage. This feature effectively avoids damage to the battery if the charger was programmed with invalid data.

Based on the presence or absence of the AC adapter, the MAX1535A automatically selects the appropriate source for supplying power to the system. A P-channel load switch controlled from the PDL output and a similar P-channel source switch controlled from the PDS output are used to implement this function. The MAX1535A can be programmed by a microcontroller (µC) to perform a relearning, or conditioning, cycle in which the battery is isolated from the charger and completely discharged through the system load. When the battery reaches 100% depth of discharge, it is recharged to full capacity (contact the battery-pack manufacturers for the 100% depth of discharge threshold).

The circuit shown in Figure 1 demonstrates a typical application for smart-battery systems.

Setting Charge Voltage

The SMBus specification allows for a 16-bit ChargeVoltage() command that translates to a 1mV LSB and a 65.535V full-scale voltage; therefore, the ChargeVoltage() code corresponds to the output voltage in millivolts. The MAX1535A ignores the first 4 LSBs, and uses the next 11 bits to control the voltage DAC. The charge voltage range of the MAX1535A is 0 to 19.200V. All codes requesting charge voltage greater than 19.200V result in a voltage setting of 19.200V. All codes requesting charge voltage below 1.024V result in a voltage set point of zero, which terminates charging.

The VMAX pin can be used to set an upper limit to the charge voltage. This feature supercedes the value set with the ChargeVoltage() command when charge voltage is greater than V_{CHARGE_MAX}. The voltage range of VMAX is from 0 to V_{REF}. The maximum charge voltage can be related to the voltage on VMAX using the following equation:

$$V_{CHARGE_MAX} = \frac{5V}{V} \times V_{VMAX}$$

where V_{VMAX} is the voltage on the VMAX pin.

Setting Charge Current

The SMBus specification allows for a 16-bit ChargeCurrent() command that translates to a 1mA LSB and a 65.535A full-scale current using a 10mΩ current-sense resistor (R2 in Figure 1). Equivalently, the ChargeCurrent() value sets the voltage across CSIP and CSIN inputs in 10µV per LSB increment. The MAX1535A ignores the first 7 LSBs and uses the next 6 bits to control the current DAC. The charge-current range of the MAX1535A is 0 to 8.064A using a 10mΩ current-sense resistor. All codes requesting charge current above 8.064A result in a current setting of 8.064A. All codes requesting charge current between 1mA to 128mA result in a current setting of 128mA. The default charge-current setting at power-on reset (POR) is also 128mA.

The IMAX pin can be used to set an upper limit to the charge current. This feature supercedes the value set with the ChargeCurrent() command when charge current is greater than I_{CHARGE_MAX}. The voltage range of IMAX is from 0 to V_{REF}. The maximum charge current can be related to the voltage on IMAX using the following equation:

$$I_{CHARGE_MAX} = \frac{5A}{V} \times V_{IMAX}$$

where V_{IMAX} is the voltage on the IMAX pin.

Highly Integrated Level 2 SMBus Battery Charger

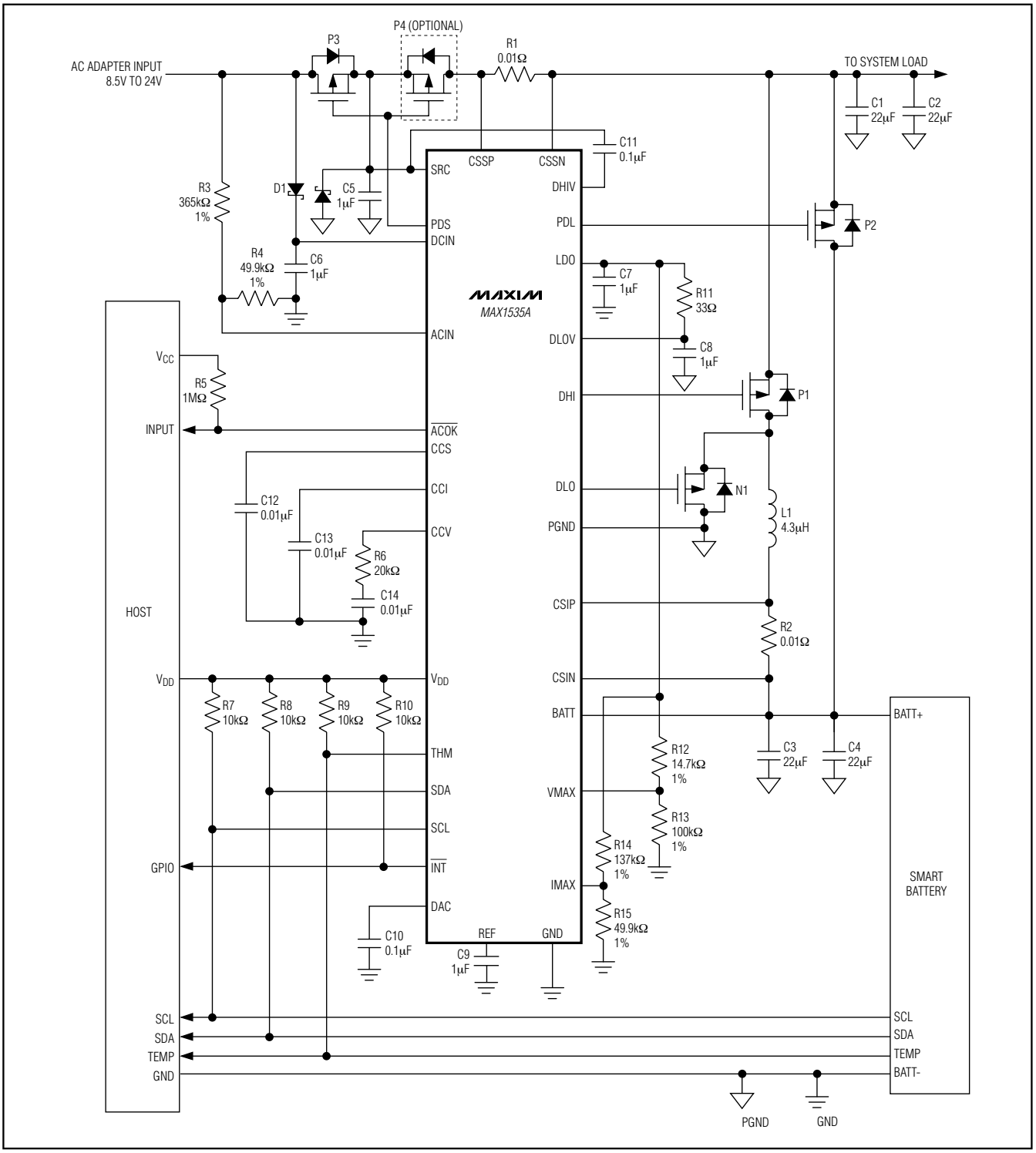


Figure 1. Standard Application Circuit

Table 1. Summary of Operating States

INPUT CONDITIONS	OPERATING STATES				
	AC PRESENT	POWER FAIL	BATTERY	BATT UNDERVOLTAGE	V_{DD} UNDERVOLTAGE
DCIN	$V_{DCIN} > 7.5V$	$V_{DCIN} < V_{BATT} + 0.3V$	X	X	X
THM	X	X	$V_{THM} < 0.91 \times V_{DD}$	X	X
BATT	X	$V_{BATT} > V_{DCIN} - 0.3V$	X	$V_{BATT} < 2.5V$	X
V_{DD}	X	X	X	X	$V_{DD} < 2.5V$

X = *Don't care.*

Setting Input-Current Limit

The total input current, from a wall cube or other DC source, is the sum of the system supply current and the current required by the charger. The MAX1535A reduces the source current by decreasing the maximum charge current when the input current exceeds the set input current limit. This technique does not truly limit the input current. As the system supply current rises, the available charge current drops proportionally to zero. Thereafter, the total input current can increase without limit.

An internal amplifier compares the differential voltage between CSSP and CSSN to a scaled voltage set by the InputCurrent() command over the SMBus. The total input current is the sum of the device supply current, the charger input current, and the system load current. The device supply current is minimal (6mA, max) in comparison to the charger current and system load. The total input current can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \left[\left(I_{CHARGE} \times V_{BATT}\right)/\left(V_{IN} \times \eta\right)\right]$$

where η is the efficiency of the DC-to-DC converter (typically 85% to 95%).

The MAX1535A allows for a 16-bit InputCurrent() command that translates to a 1mA LSB and a 65.535A full-scale current using a 10mΩ current-sense resistor (R1 in Figure 1). Equivalently, the InputCurrent() value sets the voltage across CSSP and CSSN inputs in 10µV per LSB increments. The MAX1535A ignores the first 7 LSBs and uses the next 6 bits to control the input-current DAC. The input-current range of the MAX1535A is from 256mA to 11.004A. All codes requesting input current above 11.004A result in an input-current setting of 11.004A. All codes requesting input current between 1mA to 256mA result in an input-current setting of 256mA. The default input-current-limit setting at POR is 256mA. When choosing the current-sense resistor R1, carefully calculate its power rating. Take into account variations in the system's load current and the overall accuracy of the sense amplifier. Note that the voltage drop across R1 contributes additional power loss, which reduces efficiency.

System currents normally fluctuate as portions of the system are powered up or put to sleep. Without input-current regulation, the input source must be able to deliver the maximum system current and the maximum charger-input current. By using the input-current-limit circuit, the output-current capability of the AC wall adapter can be lowered, reducing system cost.

LDO Regulator

An integrated low dropout (LDO) linear regulator provides a 5.4V supply derived from DCIN, which can deliver at least 10mA of load current. The LDO powers the gate driver of the low-side N-channel MOSFET in the DC-to-DC converter. See the *MOSFET Drivers* section. The LDO also biases the 4.096V reference and most of the control circuitry. Bypass LDO to GND with a 1µF ceramic capacitor.

V_{DD} Supply

The V_{DD} input provides power to the SMBus interface and the thermistor comparators. Connect V_{DD} to LDO, or apply an external supply to V_{DD} to keep the SMBus interface active while the supply to DCIN is removed.

Operating Conditions

Table 1 is a summary of the following four MAX1535A operating states:

- AC present. When DCIN is greater than 7.5V, the AC adapter is considered to be present. In this condition, both the LDO and REF function properly and battery charging is allowed. The AC_PRESENT bit (bit 15) in the ChargerStatus() register is set to 1.
- Power fail. When DCIN is less than BATT + 0.3V, the part is in the power-fail state since the charger does not have enough input voltage to charge the battery.

Highly Integrated Level 2 SMBus Battery Charger

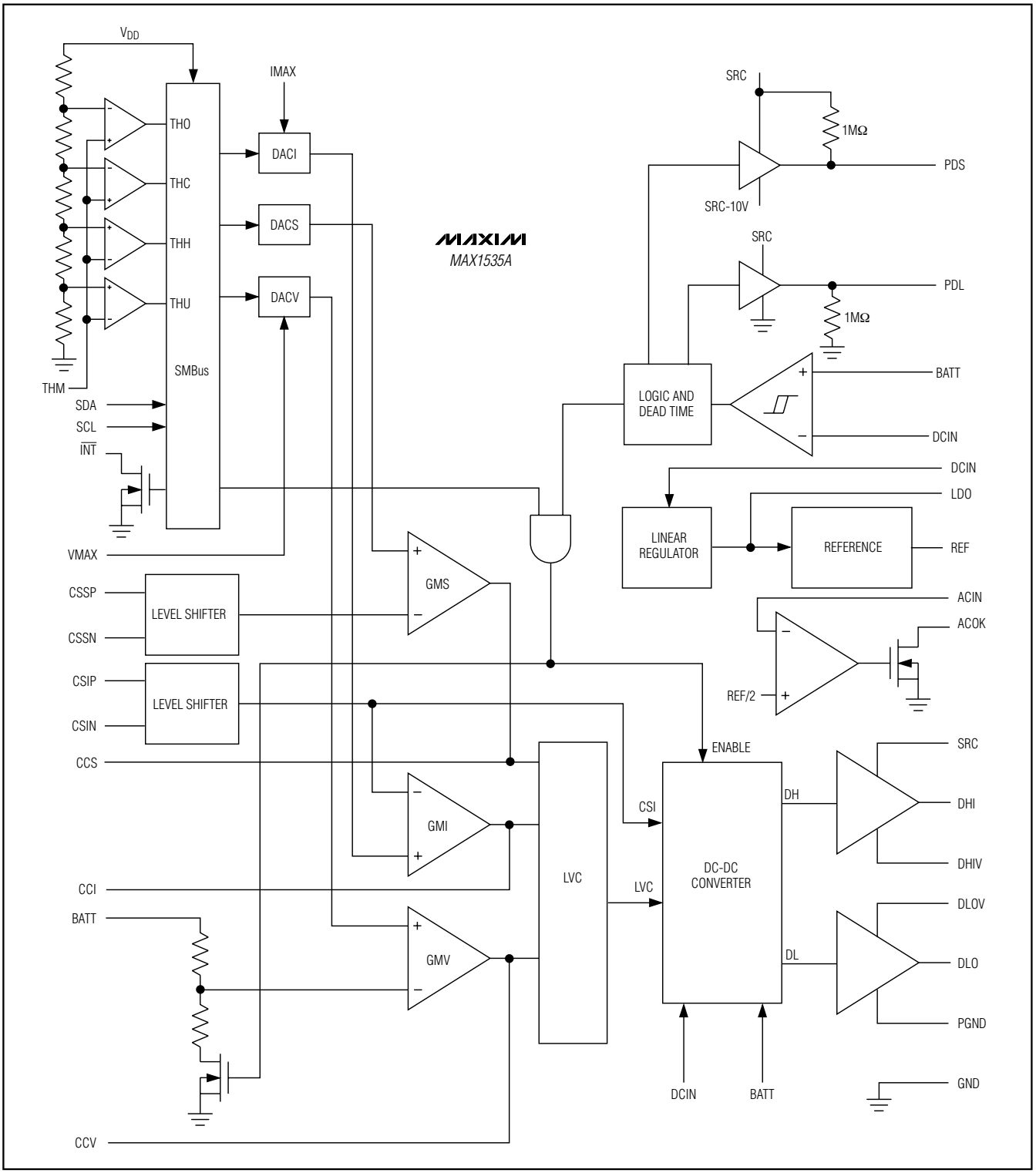


Figure 2. System Functional Diagram

In power fail, PDS turns off the input P-channel MOSFET switch and the POWER_FAIL bit (bit 13) in the ChargerStatus() register is set to 1.

- Battery present. When THM is less than 91% of V_{DD}, the battery is considered to be present. The MAX1535A uses the THM pin to detect whether a battery is connected to the charger. When the battery is present, the BATTERY_PRESENT bit (bit 14) in the ChargerStatus() register is set to 1.
- Battery undervoltage. When BATT is less than 2.5V, the battery is considered to be in an undervoltage state. This condition causes the charger to reduce its current compliance to 128mA. The content of the ChargeCurrent() register is unaffected. When the BATT voltage exceeds 2.7V, normal charging resumes. ChargeVoltage() is unaffected and can be set as low as 1.024V.
- V_{DD} undervoltage. When V_{DD} is less than 2.5V, the V_{DD} supply is considered to be in an undervoltage state. The SMBus interface does not respond to commands. Coming out of the undervoltage condition, the part is in its POR state. No charging occurs when V_{DD} is in the undervoltage state.

SMBus Interface

The MAX1535A receives control inputs from the SMBus interface. The serial interface complies with the SMBus protocols as documented in System Management Bus Specification V1.1 and can be downloaded from www.sbs-forum.org. The charger functionality complies with Intel/Duracell smart charger specifications for a level 2 charger, as well as supporting input current limit and power source selection functions.

The MAX1535A uses the SMBus Read-Word and Write-Word protocols (Figure 3) to communicate with the bat-

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 bits	1b	1b	8 bits	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

Preset to 0b0001001

ChargerMode() = 0x12
ChargeCurrent() = 0x14
ChargeVoltage() = 0x15
AlarmWarning() = 0x16
InputCurrent() = 0x3F

D7 D0 D15 D8

b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

Preset to 0b0001001

ChargerSpecInfo() = 0x11
ChargerStatus() = 0x13

Preset to 0b0001001

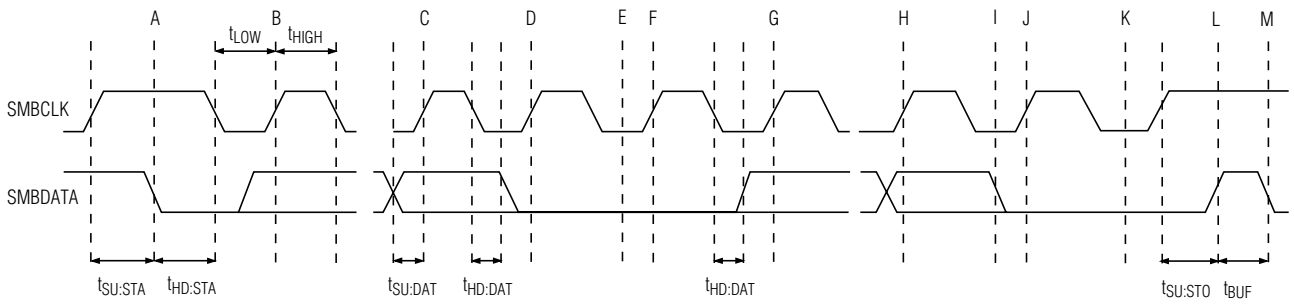
D7 D0 D15 D8

LEGEND:
S = START CONDITION or REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC LOW)
W = WRITE BIT (LOGIC LOW)
P = Stop Condition
NACK = NOT ACKNOWLEDGE (LOGIC HIGH)
R = READ BIT (LOGIC HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 3. SMBus a) Write-Word and b) Read-Word Protocols

Highly Integrated Level 2 SMBus Battery Charger

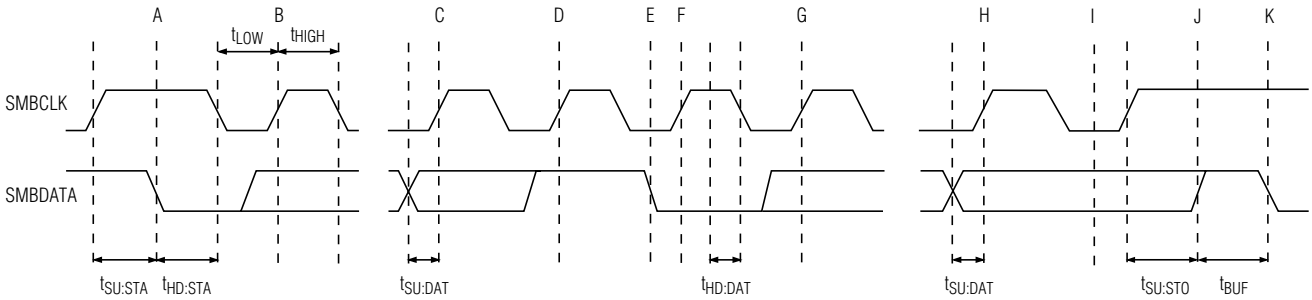


A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW

F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE
H = LSB OF DATA CLOCKED INTO SLAVE
I = SLAVE PULLS SMBDATA LINE LOW

J = ACKNOWLEDGE CLOCKED INTO MASTER
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION, DATA EXECUTED BY SLAVE
M = NEW START CONDITION

Figure 4. SMBus Write Timing



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE

E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO MASTER
H = LSB OF DATA CLOCKED INTO MASTER

I = ACKNOWLEDGE CLOCK PULSE
J = STOP CONDITION
K = NEW START CONDITION

Figure 5. SMBus Read Timing

tery being charged, as well as with any host system that monitors the battery-to-charger communications as a level 2 SMBus charger. The MAX1535A is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001. In addition, the MAX1535A has two identification (ID) registers: a 16-bit device ID register (0x0006), and a 16-bit manufacturer ID register (0x004D).

The data input SDA and clock input SCL pins have Schmitt-trigger inputs that can accommodate slow edges; however, the rising and falling edges should still be faster than 1µs and 300ns, respectively.

Communication starts with the master signaling the beginning of a transmission with a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figures 4 and 5 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data byte are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START

and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX1535A since either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. The MAX1535A supports the charger commands as described in Tables 2–9.

Battery-Charger Commands

The MAX1535A supports seven battery charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2.

ChargerSpec()

The ChargerSpec() command uses the Read-Word protocol (Figure 3). The command code for ChargerSpec() is 0x11(0b00010001). Table 3 lists the functions of the data bits (D0–D15). Bit 0 refers to the D0 bit in the Read-Word protocol. The MAX1535A complies with Level 2 Smart-Battery Charger Specification Revision 1.1; therefore, the ChargerSpec() command returns 0x0002.

ChargerMode()

The ChargerMode() command uses the Write-Word protocol (Figure 3). The command code for ChargerMode() is 0x12 (0b00010010). Table 4 lists the functions of the data bits (D0–D15). Bit 0 refers to the D0 bit in the Write-Word protocol.

To charge a battery that has a thermistor impedance in the HOT range (i.e., THERMISTOR_HOT = 1 and THERMISTOR_UR = 0), the host must use the ChargerMode() command to clear HOT_STOP after the battery is inserted. The HOT_STOP bit returns to its default power-up condition (1) whenever the battery is removed.

ChargerStatus()

The ChargerStatus() command uses the Read-Word protocol (Figure 3). The command code for ChargerStatus() is 0x13 (0b00010011). Table 5 describes the functions of the data bits (D0–D15). Bit 0 refers to the D0 bit in the Read-Word protocol.

The ChargerStatus() command returns information about thermistor impedance and the MAX1535A's internal state. The latched bits, THERMISTOR_HOT and ALARM_INHIBITED, are cleared whenever BATTERY_PRESENT = 0 or ChargerMode() is written with POR_RESET = 1. The ALARM_INHIBITED status bit can also be cleared by writing a new charge current or charge voltage.

ChargeCurrent() (POR: 0x0080)

The ChargeCurrent() command uses the Write-Word protocol (Figure 3). The command code for ChargeCurrent() is 0x14 (0b00010100). The 16-bit binary number formed by D15–D0 represents the charge-current set point in milliamps. However, the resolution of the MAX1535A is 128mA in setting the charge current; bits D0–D6 are ignored as shown in Table 6. The D13, D14, and D15 bits are also ignored. Figure 6 shows the mapping between the charge-current set point and the ChargeCurrent() code. All codes requesting charge current above 8.064A result in a current overrange, limiting the charging current to 8.064A. All codes requesting charge current between 1mA to 128mA result in a current setting of 128mA. A 10mΩ current-sense resistor (R2 in Figure 1) is required to achieve the correct code/current scaling.

Table 2. Battery-Charger Command Summary

COMMAND	COMMAND NAME	READ/WRITE	DESCRIPTION	POR STATE	STATUS BITS AFFECTED
0x11	ChargerSpec()	Read Only	Charger specification	0x0002	N/A
0x12	ChargerMode()	Write Only	Charger mode	N/A	CHARGE_INHIBITED, ALARM_INHIBITED, THERMISTOR_HOT
0x13	ChargerStatus()	Read Only	Charger status	N/A	N/A
0x14	ChargeCurrent()	Write Only	Charge-current setting	0x0080	CURRENT_NOT_REG, CURRENT_OR
0x15	ChargeVoltage()	Write Only	Charge-voltage setting	0x4B00	VOLTAGE_NOT_REG, VOLTAGE_OR
0x16	AlarmWarning()	Write Only	Alarm warning	N/A	N/A
0x3F	InputCurrent()	Write Only	Input current-limit setting	0x0080	CURRENT_NOT_REG
0xFE	DeviceID()	Read Only	Device ID	0x0006	N/A
0xFF	ManufacturerID()	Read Only	Manufacturer ID	0x004D	N/A

Table 3. ChargerSpec()

BIT	BIT NAME	DESCRIPTION
0	CHARGER_SPEC	Returns a zero for version 1.1
1	CHARGER_SPEC	Returns a 1 for version 1.1
2	CHARGER_SPEC	Returns a zero for version 1.1
3	CHARGER_SPEC	Returns a zero for version 1.1
4	SELECTOR_SUPPORT	Returns a zero, indicating no smart-battery selector functionality
5	Reserved	Returns a zero
6	Reserved	Returns a zero
7	Reserved	Returns a zero
8	Reserved	Returns a zero
9	Reserved	Returns a zero
10	Reserved	Returns a zero
11	Reserved	Returns a zero
12	Reserved	Returns a zero
13	Reserved	Returns a zero
14	Reserved	Returns a zero
15	Reserved	Returns a zero

Command: 0x11

The default charge-current setting at POR is 128mA. Thus, the first time a MAX1535A powers up, the charge current is regulated at 128mA. Anytime the battery is removed, the ChargeCurrent() register returns to its POR state.

ChargeVoltage() (POR: 0x4B00)

The ChargeVoltage() command uses the Write-Word protocol (Figure 3). The command code for ChargeVoltage() is 0x15 (0b00010101). The 16-bit binary number formed by D15–D0 represents the charge-voltage set point in millivolts. However, the resolution of the MAX1535A is 16mV in setting the charge voltage; the D0–D3 bits are ignored as shown in Table 7. The D15 bit is also ignored. Figure 7 shows the mapping between the charge-voltage set point and the ChargeVoltage() code. All codes requesting charge voltage greater than 19.200V result in a voltage overrange, limiting the charge voltage to 19.200V. All codes requesting charge voltage below 1024mV result in a voltage set point of zero, which terminates charging.

The default charge-voltage setting at POR is 19.200V. Thus, the first time a MAX1535A powers up, the charge voltage is regulated at 19.200V. Anytime the battery is removed, the ChargeVoltage() register returns to its POR state.

AlarmWarning()

The AlarmWarning() command uses the Write-Word protocol (Figure 3). The command code for AlarmWarning() is 0x16 (0b00010110). AlarmWarning() sets the ALARM_INHIBITED status bit in the MAX1535A if D15, D14, D13, D12, or D11 of the Write-Word protocol equals 1. Table 8 summarizes the AlarmWarning() command's function. The ALARM_INHIBITED status bit remains set until the battery is removed, a ChargerMode() command is written with the POR_RESET bit set, or new ChargeCurrent() and ChargeVoltage() values are written. As long as ALARM_INHIBITED = 1, the MAX1535A switching regulator remains off.

InputCurrent() (POR: 0x0080)

The InputCurrent() command uses the Write-Word protocol (Figure 3). The command code for InputCurrent() is 0x3F (0b00111111). The 16-bit binary number formed by D15–D0 represents the charge-current set point in milliamps. However, the resolution of the MAX1535A is 256mA in setting the charge current; the D0–D6 bits are ignored as shown in Table 9. The D13, D14, and D15 bits are also ignored. Figure 8 shows the mapping between the input-current set point and the InputCurrent() code. All codes requesting input current greater than 11.004A result in an input-current overrange, limiting the input current to 11.004A. All codes requesting input current between 1mA and 256mA

Table 4. ChargerMode()

BIT	BIT NAME	DESCRIPTION
0	INHIBIT_CHARGE	0* = Allow normal operation; clear the CHG_INHIBITED flip-flop. 1 = Turn off the charger; set the CHG_INHIBITED flip-flop. The CHG_INHIBITED flip-flop is not affected by any other commands.
1	ENABLE_POLLING	Not implemented
2	POR_RESET	0* = No change. 1 = Change the ChargeVoltage() to 0x4B00 and the ChargeCurrent() to 0x0080; clear the THERMISTOR_HOT and ALARM_INHIBITED flip-flops.
3	RESET_TO_ZERO	0* = No change. 1 = Set the ChargeCurrent() and ChargeVoltage() to zero even if the INHIBITED_CHARGE bit is zero.
4	AC_PRESENT_MASK	0* = Interrupt on either edge of the AC_PRESENT status bit. 1 = Do not interrupt because of an AC_PRESENT bit change.
5	BATTERY_PRESENT_MASK	0* = Interrupt on either edge of the BATTERY_PRESENT status bit. 1 = Do not interrupt because of a BATTERY_PRESENT bit change.
6	POWER_FAIL_MASK	0* = Interrupt on either edge of the POWER_FAIL status bit. 1 = Do not interrupt because of a POWER_FAIL bit change.
7	—	Not implemented
8	CALIBRATION_ENABLE	0* = When DCIN > BATT + 100mV, PDS pulls low and PDL pulls high. 0 = When DCIN < BATT + 100mV, PDS pulls high and PDL pulls low. 1 = When THM < 91% and DCIN > BATT + 100mV, PDS pulls high and PDL pulls low. 1 = When THM > 91% and DCIN > BATT + 100mV, PDS pulls high and PDL pulls low.
9	—	Not implemented
10	HOT_STOP	0 = The THERMISTOR_HOT status bit does not turn off the charger. 1* = The THERMISTOR_HOT status bit does turn off the charger. THERMISTOR_HOT is reset by either POR_RESET or BATTERY_PRESENT = 0.
11	—	Not implemented
12	—	Not implemented
13	—	Not implemented
14	—	Not implemented
15	—	Not implemented

Command: 0x12

** Indicates POR state.*

result in a current setting of 256mA. A 10mΩ current-sense resistor (R1 in Figure 1) is required to achieve the correct code/current scaling.

The default input current-limit setting at POR is 256mA. Thus, the first time a MAX1535A powers up, the input current is limited to 256mA. Anytime the battery is removed, the InputCurrent() register returns to its POR state.

Interrupts and Alert Response Address

The MAX1535A requests an interrupt by pulling the $\overline{INT}$ pin low. An interrupt is normally requested when there is a change in the state of the ChargerStatus() bits POWER_FAIL (bit 13), BATTERY_PRESENT (bit 14), or AC_PRESENT (bit 15). Therefore, the $\overline{INT}$ pin pulls low whenever the AC adapter is connected or disconnected, the battery is inserted or removed,

Highly Integrated Level 2 SMBus Battery Charger

Table 5. ChargerStatus()

BIT	BIT NAME	DESCRIPTION
0	CHARGE_INHIBITED	0* = Ready to charge the smart battery. 1 = Charging is inhibited; charge current is 0mA. This status bit returns the value of the CHG_INHIBITED flip-flop.
1	MASTER_MODE	Always returns a zero
2	VOLTAGE_NOT_REG	0 = Battery voltage is limited at the set point. 1 = Battery voltage is less than the set point.
3	CURRENT_NOT_REG	0 = Battery current is limited at the set point. 1 = Battery current is less than the set point.
4	LEVEL_2	Always returns a 1
5	LEVEL_3	Always returns a zero
6	CURRENT_OR	0 = The ChargeCurrent() value is valid for the MAX1535A. 1 = The ChargeCurrent() value exceeds the MAX1535A output range, i.e., programmed ChargeCurrent() exceeds 0x1F80.
7	VOLTAGE_OR	0 = The ChargeVoltage() value is valid for the MAX1535A. 1 = The ChargeVoltage() value exceeds the MAX1535A output range, i.e., programmed ChargeVoltage() exceeds 0x4B00.
8	THERMISTOR_OR	0 = THM is < 91% of V_{DD}. 1 = THM is > 91% of V_{DD}.
9	THERMISTOR_COLD	0 = THM is < 75% of V_{DD}. 1 = THM is > 75% of V_{DD}.
10	THERMISTOR_HOT	0 = THM has not dropped to < 23% of V_{DD}. 1 = THM has dropped to < 23% of V_{DD}. THERMISTOR_HOT flip-flop cleared by BATTERY_PRESENT = 0 or writing a 1 into the POR_RESET bit in the ChargerMode() command.
11	THERMISTOR_UR	0 = THM is > 5% of V_{DD}. 1 = THM is < 5% of V_{DD}.
12	ALARM_INHIBITED	Returns the state of the ALARM_INHIBITED flip-flop. This flip-flop is set by either a watchdog timeout or by writing an AlarmWarning() command with bits 12, 14, or 15 set. This flip-flop is cleared by BATTERY_PRESENT = 0, or writing a 1 into the POR_RESET bit in the ChargerMode() command, or by receiving successive ChargeVoltage() and ChargeCurrent() commands.
13	POWER_FAIL	0 = ACIN is above the REF/2 threshold. 1 = ACIN is below the REF/2 threshold.
14	BATTERY_PRESENT	0 = No battery is present ($V_{THM} > 0.91 \times V_{DD}$). 1 = Battery is present ($V_{THM} < 0.91 \times V_{DD}$).
15	AC_PRESENT	0 = DCIN is below the 7.5V undervoltage threshold. 1 = DCIN is above the 7.5V undervoltage threshold.

Command: 0x13

** Indicates POR state.*

Table 6. ChargeCurrent()

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mA weight.
1	—	Not used. Normally a 2mA weight.
2	—	Not used. Normally a 4mA weight.
3	—	Not used. Normally an 8mA weight.
4	—	Not used. Normally a 16mA weight.
5	—	Not used. Normally a 32mA weight.
6	—	Not used. Normally a 64mA weight.
7	Charge Current, DACI 0	0 = Adds 0mA of charger-current compliance. 1 = Adds 128mA of charger-current compliance.
8	Charge Current, DACI 1	0 = Adds 0mA of charger-current compliance. 1 = Adds 256mA of charger-current compliance.
9	Charge Current, DACI 2	0 = Adds 0mA of charger-current compliance. 1 = Adds 512mA of charger-current compliance.
10	Charge Current, DACI 3	0 = Adds 0mA of charger-current compliance. 1 = Adds 1024mA of charger-current compliance.
11	Charge Current, DACI 4	0 = Adds 0mA of charger-current compliance. 1 = Adds 2048mA of charger-current compliance, 8064mA max.
12	Charge Current, DACI 5	0 = Adds 0mA of charger-current compliance. 1 = Adds 4096mA of charger-current compliance, 8064mA max.
13	—	Not used. Normally an 8192mA weight.
14	—	Not used. Normally a 16384mA weight.
15	—	Not used. Normally a 32768mA weight.

Command: 0x14

or the charger goes in or out of dropout. The interrupts from each of the ChargerStatus() bits can be masked by an associated ChargerMode() bit POWER_FAIL_MASK (bit 6), BATTERY_PRESENT_MASK (bit 5), or AC_PRESENT_MASK (bit 4).

Interrupts are cleared by sending a command to the AlertResponse() address, 0x19, using a modified Receive-Byte protocol. In this protocol, the devices that set an interrupt try to respond by transmitting their addresses, and the devices with the highest priority or most leading zeros are recognized and cleared. This process is repeated until all devices requesting interrupts are addressed and cleared. The MAX1535A responds to the AlertResponse() address with 0x13, which is its address and a trailing 1.

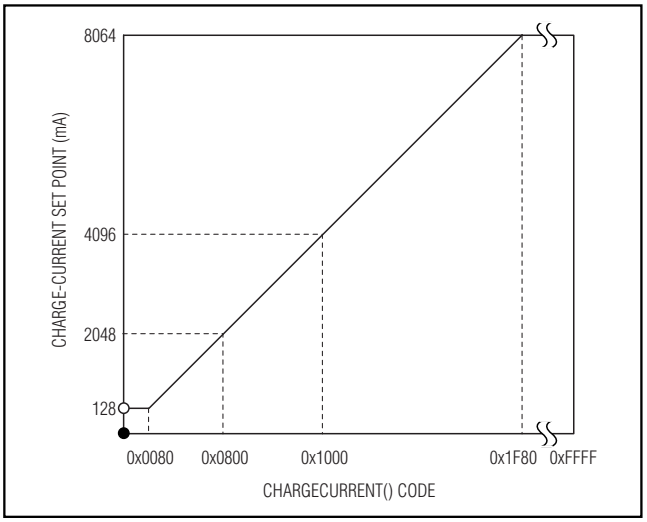


Figure 6. ChargeCurrent() Code to Charge-Current Set Point Mapping (R_2 = 10mΩ)

Highly Integrated Level 2 SMBus Battery Charger

Table 7. ChargeVoltage()

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally an 8mV weight.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charge-voltage compliance, 1024mV min. 1 = Adds 16mV of charge-voltage compliance.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charge-voltage compliance, 1024mV min. 1 = Adds 32mV of charge-voltage compliance.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charge-voltage compliance, 1024mV min. 1 = Adds 64mV of charge-voltage compliance.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charge-voltage compliance, 1024mV min. 1 = Adds 128mV of charge-voltage compliance.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charge-voltage compliance, 1024mV min. 1 = Adds 256mV of charge-voltage compliance.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charge-voltage compliance, 1024mV min. 1 = Adds 512mV of charge-voltage compliance.
10	Charge Voltage, DACV 6	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 1024mV of charge-voltage compliance.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 2048mV of charge-voltage compliance.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 4096mV of charge-voltage compliance.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 8192mV of charge-voltage compliance.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 16384mV of charge-voltage compliance, 19200mV max.
15	—	Not used. Normally a 32768mV weight.

Command: 0x15

Charger Timeout

The MAX1535A includes a timer that terminates charging if the charger has not received a ChargeVoltage() or ChargeCurrent() command in 175s. During charging, the timer is reset each time a ChargeVoltage() or ChargeCurrent() command is received; this ensures that the charging cycle is not terminated.

Thermistor Comparators

Four thermistor comparators evaluate the voltage at the THM input to determine the battery temperature. This input is meant to be used with the internal thermistor connected to ground inside the battery pack. Connect the output of the battery thermistor to THM. Connect a pullup resistor from THM to V_{DD}. The resistive voltage-divider sets the voltage at THM.

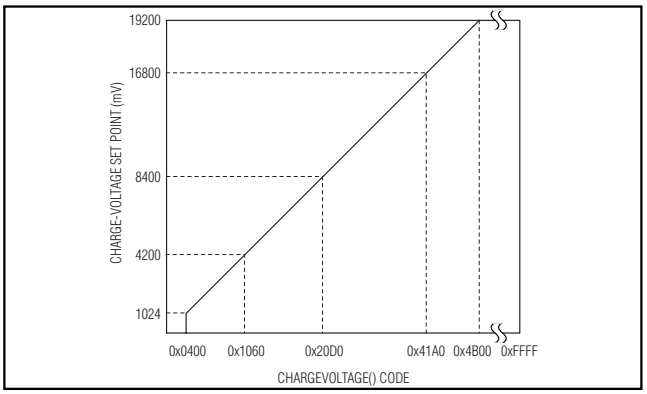


Figure 7. ChargeVoltage() Code to Charge-Voltage Set Point Mapping

Table 8. AlarmWarning()

BIT	BIT NAME	DESCRIPTION
0	Error Code	Not used
1	Error Code	Not used
2	Error Code	Not used
3	Error Code	Not used
4	FULLY_DISCHARGED	Not used
5	FULLY_CHARGED	Not used
6	DISCHARGING	Not used
7	INITIALIZING	Not used
8	REMAINING_TIME_ALARM	Not used
9	REMAINING_CAPACITY_ALARM	Not used
10	Reserved	Not used
11	TERMINATE_DISCHARGE_ALARM	Not used
12	OVER_TEMP_ALARM	0 = Charge normally. 1 = Terminate charging.
13	OTHER_ALARM	0 = Charge normally. 1 = Terminate charging.
14	TERMINATE_CHARGE_ALARM	0 = Charge normally. 1 = Terminate charging.
15	OVER_CHARGE_ALARM	0 = Charge normally. 1 = Terminate charging.

Command: 0x16

Thermistor Bits

Table 10 summarizes the conditions for setting the thermistor bits and how these 4 bits affect the charging status when a 10kΩ pullup resistor is connected between V_{DD} and THM:

- THERMISTOR_OR bit is set when the thermistor value is greater than 100kΩ. This indicates that the thermistor is open or a battery is not present. The charger is set to POR, and the BATTERY_PRESENT bit is cleared.
- THERMISTOR_COLD bit is set when the thermistor value is greater than 30kΩ. The thermistor indicates a cold battery. This bit does not affect charging.
- THERMISTOR_HOT bit is set when the thermistor value is less than 3kΩ. This is a latched bit and is cleared by removing the battery or sending a POR with the ChargerMode() command. The charger is terminated unless the HOT_STOP bit is cleared in the ChargerMode() command or the THERMISTOR_UR bit is set. See Tables 4 and 10.
- THERMISTOR_UR bit is set when the thermistor value is less than 500Ω (i.e., THM is grounded).

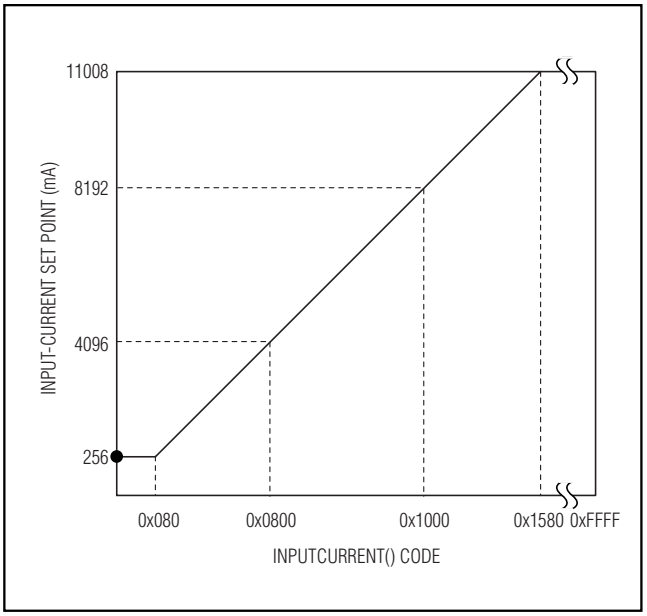


Figure 8. InputCurrent() Code to Input Current-Limit Mapping

Highly Integrated Level 2 SMBus Battery Charger

Multiple bits may be set depending on the value of the thermistor (e.g., a thermistor that is 450Ω causes both the THERMISTOR_HOT and the THERMISTOR_UR bits to be set). The thermistor may be replaced with fixed-value resistors in battery packs that do not require the thermistor as a secondary fail-safe indicator. In that case, it is the responsibility of the battery pack electronics to manipulate the resistance to obtain correct charger behavior.

AC Adapter Detection and Power Source Selection

The MAX1535A includes a hysteretic comparator that detects the presence of an AC power adapter. The MAX1535A automatically delivers power to the system load from an appropriate available power source. When the adapter is present, the open-drain ACOK output becomes high impedance and the P-channel source switch (P3 in Figure 1) is turned on by PDS, thereby powering the system. The switch threshold at ACIN is 2.048V. Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. When charging, the battery is isolated from the system load with the P-channel load switch (P2 in Figure 1), which is switched off by PDL. When the adapter is absent, the drive to the switches changes state in a fast break-before-make sequence. PDL begins to turn on 7.5µs after PDS begins to turn off.

The threshold for selecting between the PDL and PDS switches is set based on the voltage difference between the DCIN and the BATT pins. If this voltage difference drops below 100mV, the PDS is switched off and PDL is switched on. Under these conditions, the MAX1535A is completely powered down. The PDL switch is kept on with a 100kΩ pulldown resistor when the AC adapter is removed.

The drivers for PDL and PDS are fully integrated. The positive bias inputs for the drivers connect to the SRC pin and the negative bias inputs connect to a negative regulator referenced to SRC. With this arrangement, the drivers can swing from SRC to approximately 10V below SRC.

DC-to-DC Converter

The MAX1535A employs a synchronous step-down DC-to-DC converter with a P-channel high-side MOSFET switch and an N-channel low-side synchronous rectifier. The MAX1535A features a pseudofixed-frequency, current-mode control scheme with cycle-by-cycle current limit. The off-time is dependent upon V_{DCIN}, V_{BATT}, and a time constant, with a minimum t_{OFF} of 300ns. The MAX1535A can also operate in discontinuous conduction mode for improved light-load efficiency. The operation of the DC-to-DC controller is determined by the following four comparators as shown in the functional diagram in Figure 9:

- IMIN. Compares the control signal (LVC) against 100mV (typ). When LVC voltage is less than 100mV, the comparator output is low and a new cycle cannot start.
- CCMP. Compares LVC against the charge-current feedback signal (CSI). The comparator output is high and the high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- IMAX. Compares CSI to 2V (corresponding to 10A when R2 = 10mΩ). The comparator output is high and the high-side MOSFET on-time is terminated when CSI voltage is higher than the threshold. A new cycle cannot start until the IMAX comparator output goes low.
- ZCMP. Compares CSI to 100mV (corresponding to 500mA when R2 = 10mΩ). The comparator output is high and both MOSFETs are turned off when CSI voltage is lower than the threshold.

CCV, CCI, CCS, and LVC Control Blocks

The MAX1535A controls input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops, CCV, CCI, and CCS, are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-to-DC controller. The minimum voltage at CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other two control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section).

Continuous-Conduction Mode

With sufficient charge current, the MAX1535A inductor current never reaches zero, which is defined as continuous-conduction mode. The regulator switches at 400kHz (nominal) if it is not in dropout ($V_{BATT} < 0.88 \times V_{DCIN}$). The controller starts a new cycle by turning on the high-side P-channel MOSFET and turning off the low-side N-channel MOSFET. When the charge-current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side P-channel MOSFET and turning on the low-side N-channel MOSFET. The operating frequency is governed

Table 9. InputCurrent()

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 2mA weight.
1	—	Not used. Normally a 4mA weight.
2	—	Not used. Normally an 8mA weight.
3	—	Not used. Normally a 16mA weight.
4	—	Not used. Normally a 32mA weight.
5	—	Not used. Normally a 64mA weight.
6	—	Not used. Normally a 128mA weight.
7	Input Current, DACS 0	0 = Adds 0mA of input-current compliance. 1 = Adds 256mA of input-current compliance.
8	Input Current, DACS 1	0 = Adds 0mA of input-current compliance. 1 = Adds 512mA of input-current compliance.
9	Input Current, DACS 2	0 = Adds 0mA of input-current compliance. 1 = Adds 1024mA of input-current compliance.
10	Input Current, DACS 3	0 = Adds 0mA of input-current compliance. 1 = Adds 2048mA of input-current compliance.
11	Input Current, DACS 4	0 = Adds 0mA of input-current compliance. 1 = Adds 4096mA of input-current compliance.
12	Input Current, DACS 5	0 = Adds 0mA of input-current compliance. 1 = Adds 8192mA of input-current compliance.
13	—	Not used. Normally a 16384mA weight.
14	—	Not used. Normally a 32768mA weight.
15	—	Not used. Normally a 65536mA weight.

Command: 0x3F

Table 10. Thermistor Bit Settings

THERMISTOR STATUS BIT	DESCRIPTION	CONDITIONS	WAKE-UP CHARGE	CONTROLLED CHARGE
THERMISTOR_OR	Overrange	$R_{THM} > 100k\Omega$ or $V_{THM} > 0.91 \times V_{DD}$	Not allowed	Not allowed
THERMISTOR_COLD	Cold	$R_{THM} > 30k\Omega$ or $V_{THM} > 0.75 \times V_{DD}$	Allowed for timeout period	Allowed
(NONE)	Normal	$3k\Omega < R_{THM} < 30k\Omega$ or $0.23 \times V_{DD} < V_{THM} < 0.75 \times V_{DD}$	Allowed for timeout period	Allowed
THERMISTOR_HOT	Hot	$R_{THM} < 3k\Omega$ or $V_{THM} < 0.23 \times V_{DD}$	Not allowed	Not allowed
THERMISTOR_UR	Underrange	$R_{THM} < 500\Omega$ or $V_{THM} < 0.05 \times V_{DD}$	Allowed	Allowed

Highly Integrated Level 2 SMBus Battery Charger

by the off-time and is dependent upon V_{DCIN} and V_{BATT}. The off-time is set by the following equation:

$$t_{OFF} = 2.5\mu s \times \frac{V_{DCIN} - V_{BATT}}{V_{DCIN}}$$

The on-time can be determined using the following equation:

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}}$$

$$\text{where } I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}.$$

The switching frequency can then be calculated:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}}$$

These equations describe the controller's pseudofixed-frequency performance over the most common operating conditions.

At the end of the fixed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 100mV (IMIN comparator output is high), and the peak charge current is less than the cycle-by-cycle limit (IMAX comparator output is low). If the peak charge current exceeds the IMAX comparator threshold, the on-time is terminated. The IMAX comparator governs the maximum cycle-by-cycle current limit and is internally set to 10A (when R2 = 10mΩ). The cycle-by-cycle current limit effectively protects against sudden overcurrent faults.

If during the off-time the inductor current goes to zero, the ZCMP comparator output pulls high, turning off the low-side MOSFET. Both the high- and low-side MOSFETs are turned off until another cycle is ready to begin. The MAX1535A enters into the discontinuous conduction mode (see the *Discontinuous Conduction* section).

There is a 0.3µs minimum off-time when the (V_{DCIN} - V_{BATT}) differential becomes too small. If $V_{BATT} \geq 0.88 \times V_{DCIN}$, then the threshold for minimum off-time is reached and the off-time is fixed at 0.27µs. The switching frequency in this mode varies according to the equation:

$$f = \frac{1}{\frac{L \times I_{RIPPLE}}{(V_{CSSN} - V_{BATT})} + 0.27\mu s}$$

Discontinuous Conduction

The MAX1535A enters discontinuous-conduction mode when the output of the LVC control point falls below 100mV. For R2 = 10mΩ, this corresponds to 0.5A:

$$I_{MIN} = \frac{0.1V}{20 \times 2R2} = 0.5 \text{ A charge current for } R2 = 10m\Omega$$

In discontinuous mode, a new cycle is not started until the LVC voltage rises above 100mV. Discontinuous mode operation can occur during conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the charger is in constant-voltage mode with a nearly full battery pack.

Compensation

The charge voltage, charge current, and input current-limit regulation loops are compensated separately and independently at the CCV, CCI, and CCS pins.

CCV Loop Compensation

The simplified schematic in Figure 10 is sufficient to describe the operation of the MAX1535A when the voltage loop (CCV) is in control. The required compensation network is a pole-zero pair formed with C_{CV} and R_{CV}. The pole is necessary to roll off the voltage loop's response at low frequency. The zero is necessary to compensate the pole formed by the output capacitor and the load. R_{ESR} is the equivalent series resistance (ESR) of the charger output capacitor (C_{OUT}). R_L is the equivalent charger output load, where $R_L = \Delta V_{BATT} / \Delta I_{CHG}$. The equivalent output impedance of the GMV amplifier, R_{OGMV}, is greater than 10MΩ. The voltage amplifier transconductance, GMV = 0.125µA/mV. The DC-to-DC converter transconductance is dependent upon the charge current-sense resistor R2:

$$GM_{OUT} = \frac{1}{A_{CSI} \times R2}$$

where A_{CSI} = 20, and R2 = 0.01Ω in the typical application circuits, so GM_{OUT} = 5A/V.

The loop transfer function (LTF) is given by:

$$LTF = GM_{OUT} \times R_L \times GMV \times R_{OGMV} \times \frac{(1 + SC_{OUT} \times R_{ESR})(1 + SC_{CV} \times R_{CV})}{(1 + SC_{CV} \times R_{OGMV})(1 + SC_{OUT} \times R_L)}$$

The poles and zeros of the voltage-loop transfer function are listed from lowest to highest frequency in Table 11.

Near crossover C_{CV} is much lower impedance than R_{OGMV}. Since C_{CV} is in parallel with R_{OGMV}, C_{CV} dominates the parallel impedance near crossover.

Additionally, R_{CV} is much higher impedance than C_{CV} and dominates the series combination of R_{CV} and C_{CV}, so:

$$\frac{R_{OGMV} \times (1 + SC_{CV} \times R_{CV})}{(1 + SC_{CV} \times R_{OGMV})} \cong R_{CV}$$

C_{OUT} is also much lower impedance than R_L near crossover so the parallel impedance is mostly capacitive and:

$$\frac{R_L}{(1 + SC_{OUT} \times R_L)} \cong \frac{1}{SC_{OUT}}$$

If R_{ESR} is small enough, its associated output zero has a negligible effect near crossover and the loop-transfer function can be simplified as follows:

$$LTF = GM_{OUT} \times \frac{R_{CV}}{SC_{OUT}} GMV$$

Setting the LTF = 1 to solve for the unity-gain frequency yields:

$$f_{CO_CV} = GM_{OUT} \times GMV \times \frac{R_{CV}}{2\pi \times C_{OUT}}$$

For stability, choose a crossover frequency lower than 1/10th of the switching frequency. For example, choose a crossover frequency of 30kHz and solving for R_{CV} using the component values listed in Figure 1 yields R_{CV} = 20kΩ:

$$R_{CV} = \frac{2\pi \times C_{OUT} \times f_{CO_CV}}{GMV \times GM_{OUT}} = 10k\Omega$$

V_{BATT} = 16.8V

GMV = 0.125µA/mV

I_{CHG} = 4A

GM_{OUT} = 5A/V

C_{OUT} = 2 × 22µF

f_{OSC} = 400kHz

R_L = 0.2Ω

f_{CO_CV} = 30kHz

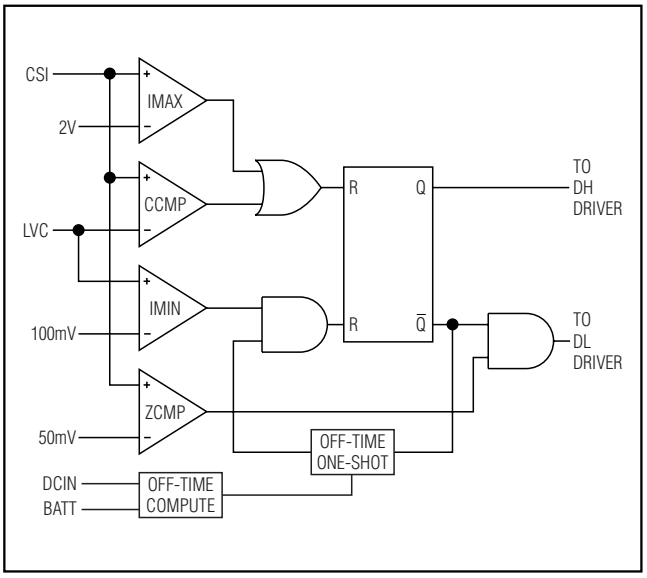


Figure 9. DC-to-DC Converter Block Diagram

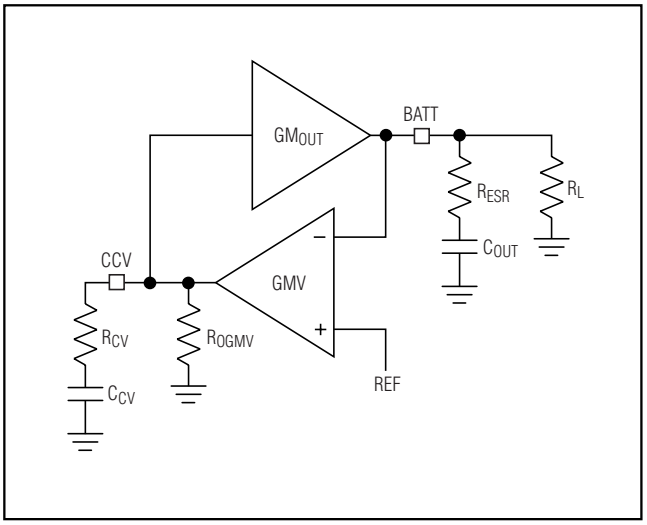


Figure 10. CCV Loop Diagram

To ensure that the compensation zero adequately cancels the output pole, select $f_{Z_CV} \le f_{P_OUT}$:

$C_{CV} \ge (R_L/R_{CV})\ C_{OUT}$

$C_{CV} \ge$ 4nF (assuming 4 cells and 4A maximum charge current)

Figure 11 shows the Bode plot of the voltage-loop frequency response using the values calculated above.

Highly Integrated Level 2 SMBus Battery Charger

Table 11. CCV Loop Poles and Zeros

NAME	EQUATION	DESCRIPTION
CCV pole	$f_{P_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CV}}$	Lowest frequency pole created by C_{CV} and GMV's finite output resistance. Since R_{OGMV} is very large and not well controlled, the exact value for the pole frequency is also not well controlled (R_{OGMV} > 10MΩ).
CCV zero	$f_{Z_CV} = \frac{1}{2\pi R_{CV} \times C_{CV}}$	Voltage-loop compensation zero. If this zero is at the same frequency or lower than the output pole f_{P_OUT}, then the loop-transfer function approximates a single-pole response near the crossover frequency. Choose C_{CV} to place this zero at least one decade below crossover to ensure adequate phase margin.
Output pole	$f_{P_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$	Output pole formed with the effective load resistance R_L and the output capacitance C_{OUT}. R_L influences the DC gain but does not affect the stability of the system or the crossover frequency.
Output zero	$f_{Z_OUT} = \frac{1}{2\pi RESR \times C_{OUT}}$	Output ESR Zero. This zero can keep the loop from crossing unity gain if f_{Z_OUT} is less than the desired crossover frequency; therefore, choose a capacitor with an ESR zero greater than the crossover frequency.

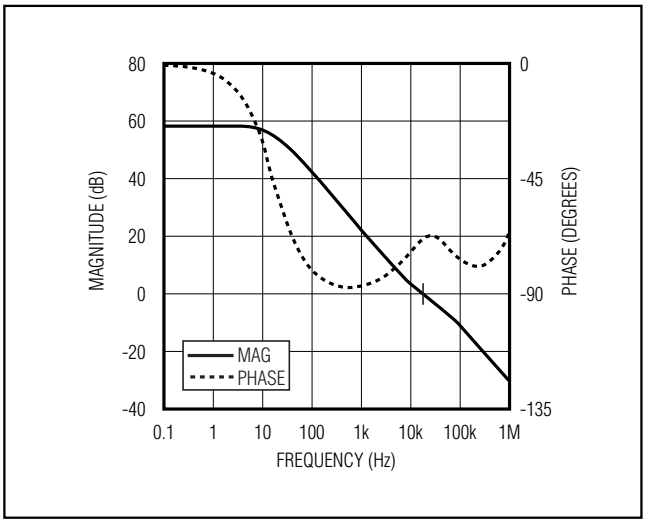


Figure 11. CCV Loop Response

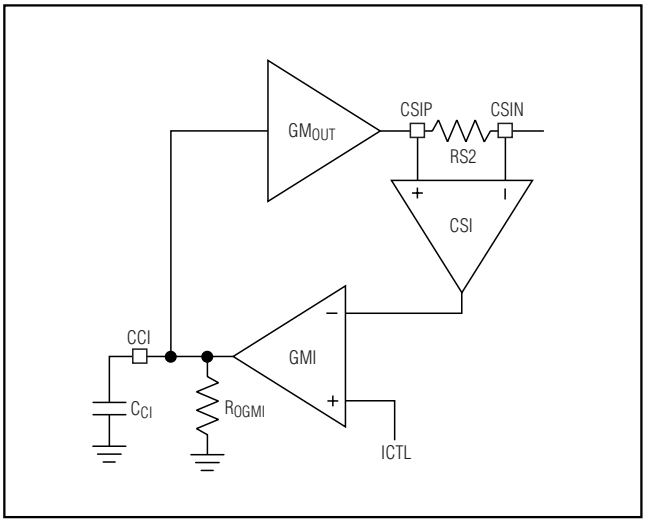


Figure 12. CCI Loop Diagram

CCI Loop Compensation

The simplified schematic in Figure 12 is sufficient to describe the operation of the MAX1535A when the battery current loop (CCI) is in control. Since the output capacitor's impedance has little effect on the response of the current loop, only a simple single pole is required to compensate this loop. A_{CSI} is the internal gain of the current-sense amplifier. R2 is the charge current-sense resistor, R2 = 10mΩ. R_{OGMI} is the equivalent output impedance of the GMI amplifier, which is greater than 10MΩ. GMI is the charge-current amplifier transconductance = 1µA/mV. GM_{OUT} is the DC-to-DC converter transconductance = 5A/V.

The loop-transfer function is given by:

$$LTF = GM_{OUT} \times A_{CSI} \times RS2 \times GMI \frac{R_{OGMI}}{1 + SR_{OGMI} \times C_{CI}}$$

This describes a single-pole system. Since:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS2}$$

the loop-transfer function simplifies to:

$$LTF = GMI \frac{R_{OGMI}}{1 + SR_{OGMI} \times C_{CI}}$$

The crossover frequency is given by:

$$f_{CO_CI} = \frac{GMI}{2\pi C_{CI}}$$

For stability, choose a crossover frequency lower than 1/10th of the switching frequency:

$$C_{CI} = GMI / (2\pi f_{CO\text{-}CI})$$

Choosing a crossover frequency of 30kHz and using the component values listed in Figure 1 yields C_{CI} > 5.4nF. Values for C_{CI} greater than 10 times the minimum value may slow down the current-loop response excessively. Figure 13 shows the Bode plot of the current-loop frequency response using the values calculated above.

CCS Loop Compensation

The simplified schematic in Figure 14 is sufficient to describe the operation of the MAX1535A when the input current-limit loop (CCS) is in control. Since the output capacitor's impedance has little effect on the response of the input current-limit loop, only a single pole is required to compensate this loop. A_{CSS} is the internal gain of the current-sense amplifier. R1 is the input current-sense resistor, R1 = 10mΩ in the typical application circuits. R_{OGMS} is the equivalent output impedance of the GMS amplifier, which is greater than 10MΩ. GMS is the charge-current amplifier transconductance = 1µA/mV. GM_{IN} is the DC-to-DC converter's input-referred transconductance = (1/D) × GM_{OUT} = (1/D) × 5A/V.

The loop-transfer function is given by:

$$LTF = GM_{IN} \times A_{CSS} \times RSI \times GMS \frac{R_{OGMS}}{1 + SR_{OGMS} \times C_{CS}}$$

Since $GM_{IN} = \frac{1}{A_{CSS} \times RS1}$, the loop – transfer function simplifies to:

$$LTF = GMS \frac{R_{OGMS}}{1 + SR_{OGMS} \times C_{CS}}$$

The crossover frequency is given by:

$$f_{CO_CS} = \frac{GMS}{2\pi C_{CS}}$$

For stability, choose a crossover frequency lower than 1/10th of the switching frequency:

$$C_{CS} = 5 \times GMS / (2\pi f_{OSC})$$

Choosing a crossover frequency of 30kHz and using the component values listed in Figure 1 yields C_{CS} > 5.4nF. Values for CCS greater than 10 times the minimum value may slow down the current-loop response excessively. Figure 15 shows the Bode plot of the input current-limit-loop frequency response using the values calculated above.

MOSFET Drivers

The DHI and DLO outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is the same for both the low-side and high-side switches. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. An adaptive dead-time circuit monitors the DLO output and prevents the high-side FET from turning on until DLO is fully off. There must be a low-resistance, low-inductance path from the DLO driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1535A interprets the MOSFET gate as "off" while there is still charge left on the gate. Use very short, wide traces measuring 10 squares to 20 squares or less (1.25mm to 2.5mm wide if the MOSFET is 25mm from the device). Unlike the DLO output, the DHI output uses a 50ns (typ) delay time to prevent the low-side MOSFET from turning on until DHI is fully off. The same layout considerations should be used for routing the DHI signal to the high-side MOSFET.

Since the transition time for a P-channel switch can be much longer than an N-channel switch, the dead time prior to the high-side P-channel MOSFET turning on is more pronounced than in other synchronous step-down regulators, which use high-side N-channel switches. On the high-to-low transition, the voltage on the inductor's "switched" terminal flies below ground until the low-side switch turns on. A similar dead-time spike occurs on the opposite low-to-high transition. Depending upon the magnitude of the load current, these spikes usually have a minor impact on efficiency.

The high-side driver (DHI) swings from SRC to 5V below SRC and has a typical impedance of 1Ω sourcing and 4Ω sinking. The low-side driver (DLO) swings

Highly Integrated Level 2 SMBus Battery Charger

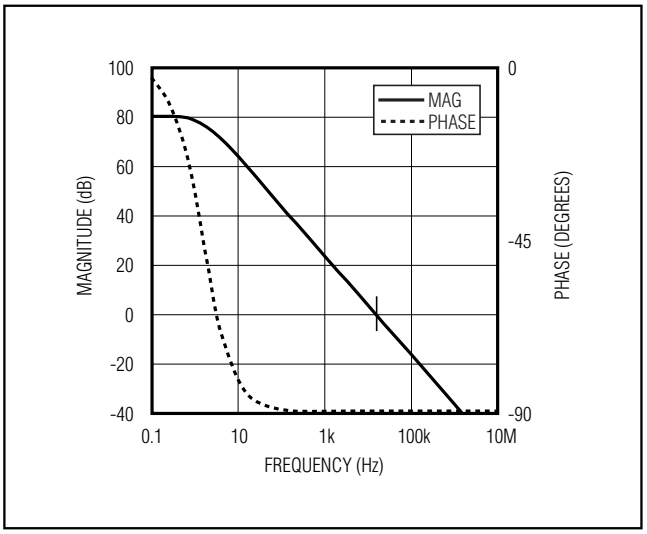


Figure 13. CCI Loop Response

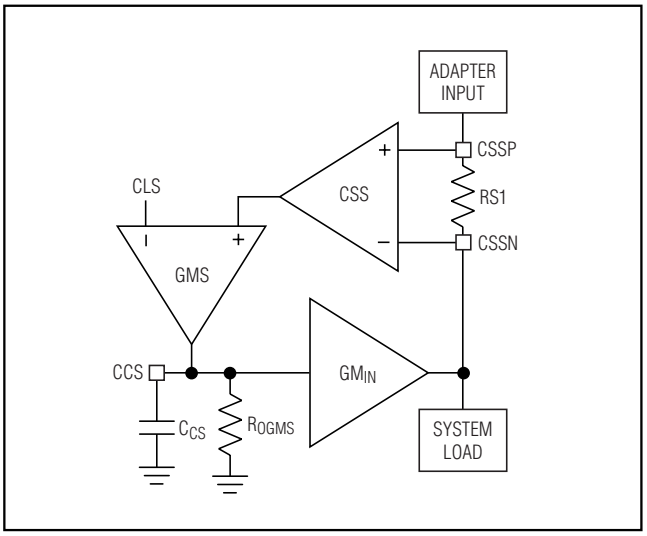


Figure 14. CCS Loop Diagram

from DLOV to ground and has a typical impedance of 1Ω sinking and 4Ω sourcing. This helps prevent DLO from being pulled up when the high-side switch turns on due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the MOSFETs that can be used. Using a low-side MOSFET with smaller gate-to-drain capacitance can prevent these problems.

Design Procedure

Table 12 lists the recommended components and refers to the circuit of Figure 1. The following sections describe how to select these components.

MOSFET Selection

MOSFETs P2 and P3 (Figure 1) provide power to the system load when the AC adapter is inserted. These devices may have modest switching speeds, but must be able to deliver the maximum input current as set by R1. As always, care should be taken not to exceed the device's maximum voltage ratings at the maximum operating temperature.

The P-channel/N-channel MOSFETs (P1, N1) are the switching devices for the step-down regulator. The guidelines for these devices focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention. The high-side MOSFET (P1) must be able to dissipate the resistive losses plus the switching losses at both $V_{DCIN(MIN)}$ and $V_{DCIN(MAX)}$. Calculate both these sums.

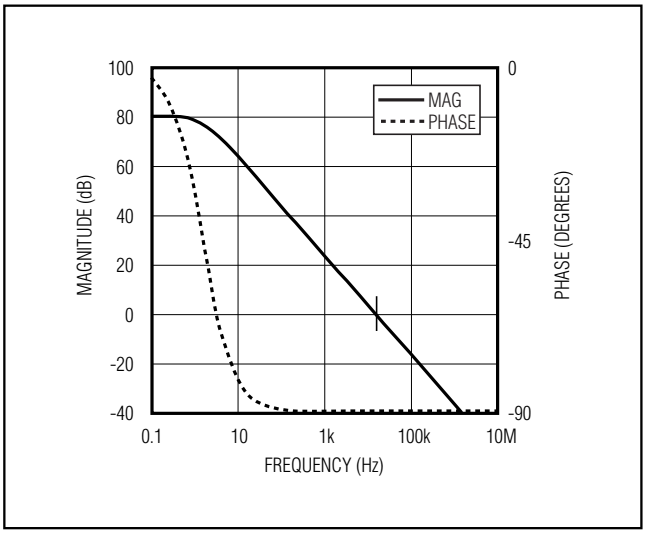


Figure 15. CCS Loop Response

Ideally, the losses at $V_{DCIN(MIN)}$ should be roughly equal to losses at $V_{DCIN(MAX)}$, with lower losses in between. If the losses at $V_{DCIN(MIN)}$ are significantly higher than the losses at $V_{DCIN(MAX)}$, consider increasing the size of P1. Conversely, if the losses at $V_{DCIN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of P1. If DCIN does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has

the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Make sure that the DLO gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

Since the MAX1535A utilizes P-channel high-side and N-channel low-side MOSFETs, the switching characteristics can be quite different. Select devices that have short turn-off times, and make sure that P1($t_{DOFF(MAX)}$) - N1($t_{DON(MIN)}$) < 40ns. Failure to do so may result in efficiency-killing shoot-through currents. If delay mismatch causes shoot-through currents, consider adding capacitance from gate to source on N1 to slow down its turn-on time.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation (PD) due to resistance occurs at the minimum supply voltage:

$$PD(HIGH\text{-}SIDE) = \left(\frac{V_{BATT}}{V_{DCIN}}\right)\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V. Calculating the power dissipation in P1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on P1:

$$PD(HS_SWITCHING) = \frac{V_{DCIN(MAX)}^2 \times C_{RSS} \times f_{SW} \times I_{LOAD}}{2 \times I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of P1, and I_{GATE} is the peak gate-drive source/sink current (4.5A sourcing and 1.1A sinking).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied due to the squared term in the C x V_{DCIN}^2 x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N1), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(LOW\text{-}SIDE) = \left[1-\left(\frac{V_{BATT}}{V_{DCIN}}\right)\right]\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{DS(ON)}$$

Choose a Schottky diode (D1, Figure 1) having a forward voltage low enough to prevent the N1 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional and can be removed if efficiency is not critical.

Inductor Selection

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 of the ripple current (ΔIL):

$$I_{SAT} = I_{CHG} + (1/2)\,\Delta IL$$

The ripple current is determined by:

$$\Delta IL = V_{BATT} \times t_{OFF} / L$$

If $V_{BATT} < 0.88V_{DCIN}$, then:

$$t_{OFF} = 2.5\mu s\,(V_{DCIN} - V_{BATT}) / V_{DCIN}$$

or:

$$t_{OFF} = 0.27\mu s \text{ (typ) for } V_{BATT} > 0.88\,V_{DCIN}$$

Figure 16 illustrates the variation of the ripple current vs. battery voltage when the circuit is charging at 3A with a fixed input voltage of 19V.

Higher inductor values decrease the ripple current. Smaller inductor values require high-saturation current capabilities and degrade efficiency. Designs that set LIR = ΔIL / I_{CHG} = 0.3 usually result in a good balance between inductor size and efficiency:

$$L = \frac{V_{BATT} \times t_{OFF}}{LIR \times I_{CHG}}$$

Highly Integrated Level 2 SMBus Battery Charger

Table 12. Recommended Components

DESIGNATION	QTY	DESCRIPTION
C1–C4	4	22µF ±20%, 25V X5R ceramic capacitors (2220) TDK C5750X5R1E226M
C5, C6	2	1µF ±10%, 25V X7R ceramic capacitors (1206) Murata GRM31MR71E105K Taiyo Yuden TMK316BJ105KL TDK C3216X7R1E105K
C7, C8, C9	3	1µF ±10%, 16V X7R ceramic capacitors (0805) Murata GRM21BR71C105K Taiyo Yuden EMK212BJ105KG TDK C2012X7R1E105K
C10, C11	2	0.1µF ±10%, 25V X7R ceramic capacitors (0603) Murata GRM188R71E104K TDK C1608X7R1E104K
C12, C13, C14	3	0.01µF ±10%, 16V X7R ceramic capacitors (0402) Murata GRP155R71E103K Taiyo Yuden EMK105BJ103KV TDK C1005X7R1E103K
D1	1	Schottky diode, 0.5A, 30V, SOD-123 Diodes Inc. B0530W General Semiconductor MBR0530 ON Semiconductor MBR0530
L1	1	4.3µH, 11A, 11.4mΩ inductor Sumida CEP125-4R3MC-U
N1	1	MOSFET, N-channel, 13.5A, +30V, 8-pin SO Fairchild FDS6670S
P1–P4	4	MOSFET, P-channel, 13A, -30V, 8-pin SO Fairchild FDS6679Z
R1, R2	2	10mΩ ±1%, 1W sense resistor (2512) IRC LRC-LRF2512-01-R010-F
R3	1	365kΩ ±1% resistor (0805)
R4	1	49.9kΩ ±1% resistor (0805)
R5	1	1MΩ 5% resistor (0805)
R6	1	20kΩ ±5% resistor (0603)
R7–R10	4	10kΩ ±5% resistors (0805)
R11	1	33Ω ±5% resistor (0805)
R12, R13	2	1MΩ potentiometers (multiturn) Bourns 3266W-1-105 or equivalent

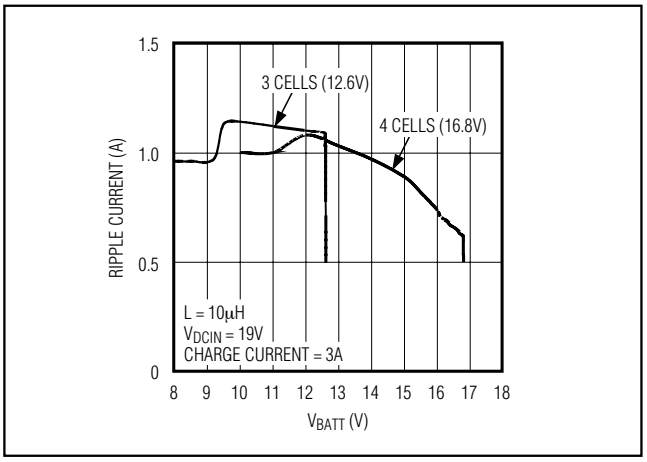


Figure 16. Ripple Current vs. Battery Voltage

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents:

$$I_{RMS} = I_{CHG}\left(\frac{\sqrt{V_{BATT}(V_{DCIN} - V_{BATT})}}{V_{DCIN}}\right)$$

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately 10°C. The maximum ripple current occurs at 50% duty factor or $V_{DCIN} = 2 \times V_{BATT}$, which equates to $0.5 \times I_{CHG}$. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions.

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to ensure the stability of the DC-to-DC converter (see the *Compensation* section.) Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents.

Applications Information

Smart-Battery System Background Information

Smart-battery systems have evolved since the conception of the smart-battery system (SBS) specifications. Originally, such systems consisted of a smart battery and smart-battery charger that were compatible with the SBS specifications and communicated directly with each other using SMBus protocols. Modern systems still employ the original commands and protocols, but often use a keyboard controller or similar digital intelligence to mediate the communication between the battery and the charger (Figure 17). This arrangement permits considerable freedom in the implementation of charging algorithms at the expense of standardization. Algorithms can vary from the simple detection of the battery with a fixed set of instructions for charging the battery to highly complex programs that can accommodate multiple battery configurations and chemistries. Microcontroller programs can perform frequent tests on the battery's state of charge and dynamically change the voltage and current applied to enhance safety. Multiple batteries can also be utilized with a selector that is programmable over the SMBus.

Batteries that use SMBus fuel gauges must sometimes perform a conditioning cycle to calibrate the fuel gauge's reference data for empty and full capacity. This cycle consists of isolating the battery from the charger and discharging it through the system load. When the battery reaches 100% depth of discharge, it is then recharged. The circuit in Figure 1 is capable of implementing this feature under software control. To utilize the conditioning function, the configuration of the PDS switch must be changed to source-connected FETs to prevent the AC adapter from supplying current to the system through the MOSFET's body diode. The SRC pin must be connected to the common source node of the back-to-back FETs to properly drive the MOSFETs.

It is essential to alert the user that the system is performing a conditioning cycle. If the user terminates the cycle prematurely, the battery may be discharged even though the system was running off an AC adapter for a substantial period of time. If the AC adapter is in fact removed during conditioning, the MAX1535A keeps the PDL switch on and the charger remains off as it would in normal operation. If the battery is removed during conditioning mode, the PDS switch is turned back on and the system is powered from the AC adapter.

Highly Integrated Level 2 SMBus Battery Charger

Setting Input Current Limit

The input current limit should be set based on the current capability of the AC adapter and the tolerance of the input current limit. The upper limit of the input current threshold should never exceed the adapter's minimum available output current. For example, if the adapter's output current rating is 5A ±10%, the input current limit should be selected so that its upper limit is less than 5A × 0.9 = 4.5A. Since the input current-limit accuracy of the MAX1535A is ±5%, the typical value of the input current limit should be set at 4.5A / 1.05 ≈ 4.28A. The lower limit for input current must also be considered. For chargers at the low end of the specification, the input current limit for this example could be 4.28A × 0.95, or approximately 4.07A.

Setting VMAX and IMAX Limits

The VMAX and IMAX limits should be determined based on the design values of the maximum current and voltage in the battery and the accuracy of VMAX and IMAX limits. The VMAX function is intended to be a secondary protection mechanism. So it is not relevant whether SMBus or VMAX controls the charger, so long as the charge voltage is below the battery manufacturer's maximum ratings. The SMBus and VMAX thresholds can therefore overlap slightly because charge-voltage accuracy is critical for safely and efficiently charging the battery. The lower limit of the VMAX threshold should be equal to the normal charge voltage of 4.20V per cell. Assuming the accuracy of the VMAX threshold is ±5%, the typical value of the VMAX limit should be set at 4.20 / 0.95 = 4.42V per cell. For a 4-cell battery pack, the nominal VMAX limit is 4 × 4.42V = 17.68V.

The accuracy of the charge current is not as critical as the charge voltage. Small variations (such as ±5%) in the absolute value of the charge current do not have a significant effect on the total charge time. It is acceptable to have the maximum charge current set by SMBus and the IMAX limit overlap slightly. Assuming the maximum charge current is 5A ±5% and the accuracy of the IMAX threshold is ±5%, the lower limit of the IMAX threshold can be set equal to the upper limit of the maximum charge current (5.25A), or slightly lower. Therefore, the typical value of the IMAX limit should be 5.25A / 0.95 = 5.53A, or slightly lower.

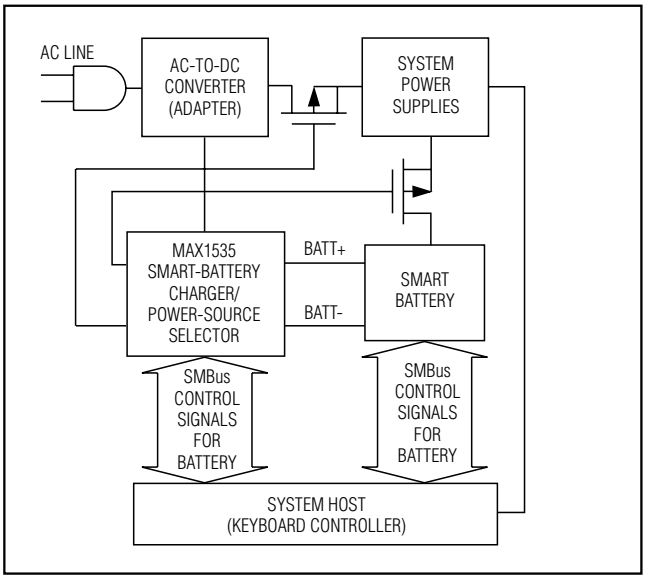


Figure 17. Typical Smart-Battery System

Layout and Bypassing

Bypass DCIN with a 1µF ceramic capacitor to ground (Figure 1). D4 protects the MAX1535A when the DC power source input is reversed. A signal diode for D1 is adequate because DCIN only powers the LDO and the internal reference. Bypass V_{DD}, DCIN, LDO, DHIV, DLOV, SRC, DAC, and REF as shown in Figure 1.

Good PC board layout is required to achieve specified noise immunity, efficiency, and stable performance. The PC board layout artist must be given explicit instructions—preferably a sketch showing the placement of the power-switching components and high-current routing. Refer to the PC board layout in the MAX1535A evaluation kit for examples. A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections, and the inner layers for uninterrupted ground planes.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:

- Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
- Minimize ground trace lengths in the high-current paths.
- Minimize other trace lengths in the high-current paths.
- Use >5mm wide traces in the high-current paths.
- Connect C1 and C2 to the high-side MOSFET (10mm, max length).
- Minimize the LX node (MOSFETs, rectifier cathode, inductor (15mm, max length)).

  Ideally, surface-mount power components are flush against each other with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and the REF capacitor). **Important**: The IC must be no further than 10mm from the current-sense resistors. Quiet connections to REF, VMAX, IMAX, CCV, CCI, CCS, ACIN, and DCIN should be returned to a separate ground (GND) island. The appropriate traces are marked on the schematic with the ground symbol. There is very little current flowing in these traces, so the ground island need not be very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low-current connections can be made through vias. The ground pad on the backside of the package should also be connected to this quiet ground island.
3) Keep the gate drive traces (DHI and DLO) as short as possible (L < 20mm), and route them away from the current-sense lines and REF. These traces should also be relatively wide (W > 1.25mm).
4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.
5) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location. See Figure 18 for a layout example.

Chip Information

TRANSISTOR COUNT: 11,900

PROCESS: BiCMOS

Highly Integrated Level 2 SMBus Battery Charger

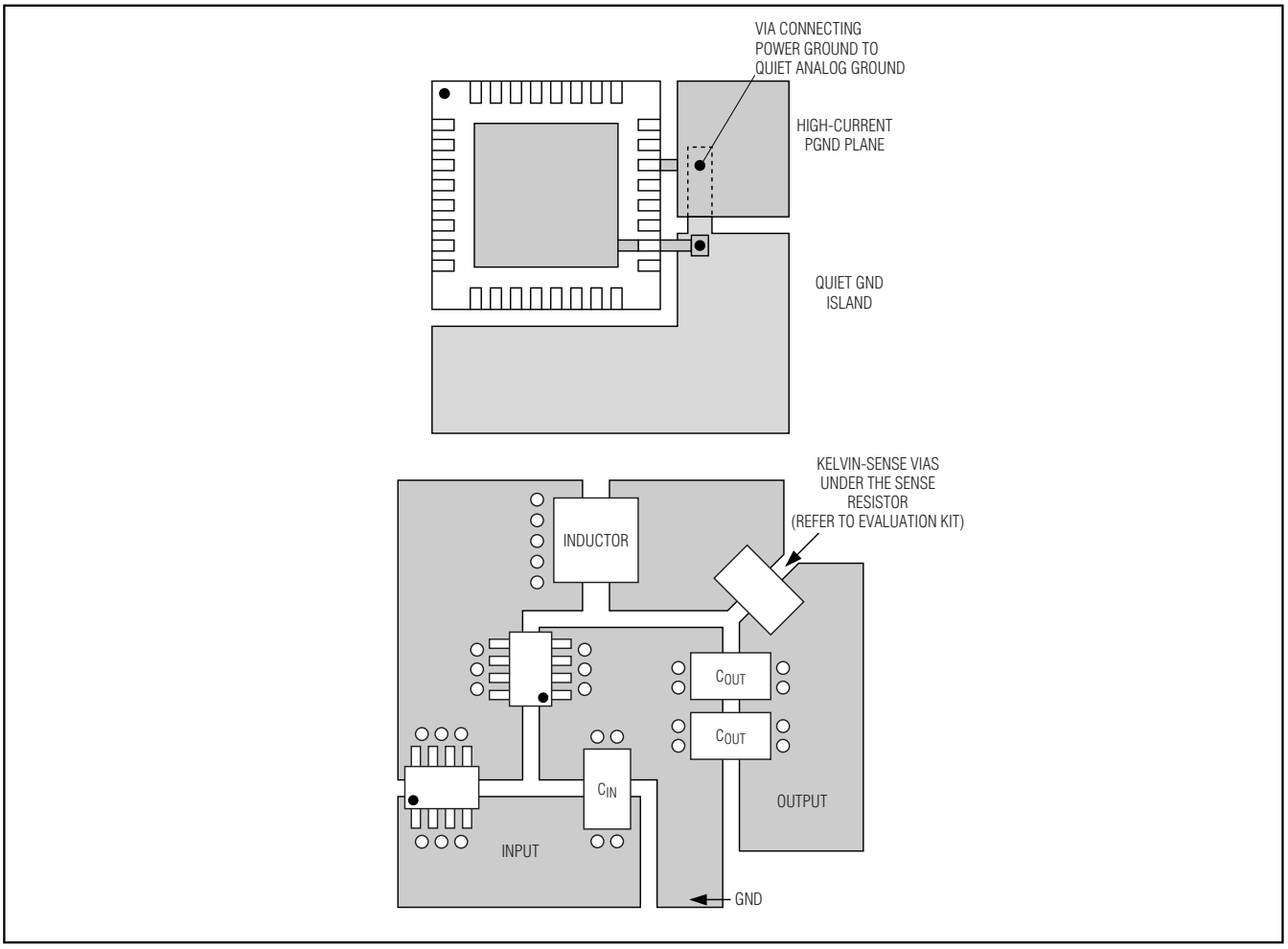
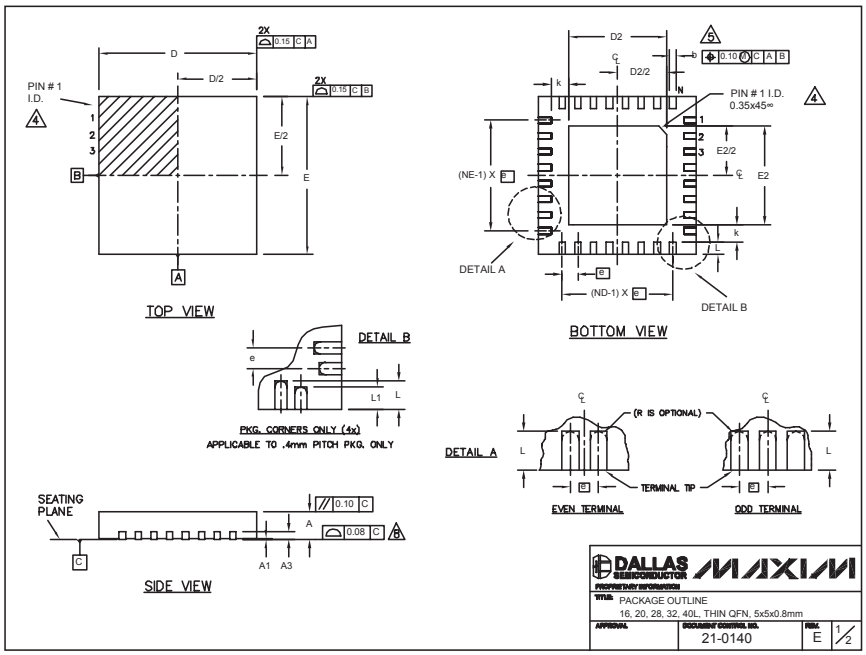


Figure 18. MAX1535A PC Board Layout Example

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	-	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	YES
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	NO
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	YES
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
16, 20, 28, 32, 40L, THIN QFN, 5x5x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. E | 2/2

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